An Integrated Folded-Patch Chip-Size Antenna Using High-Resistivity Polycrystalline Silicon Substrate

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High-resistivity polycrystalline silicon (HRPS) wafers are utilized as low-loss substrates for three-dimensional integration of on-chip antennas in wafer-level chip-scale packages (WLCSP). Sandwiching of HRPS and silicon wafers enables to integrate complex RF passives with a spacing of >150 μm to the conductive silicon substrate containing the circuitry, while providing mechanical stability, reducing form factor and avoiding any additional RF loss. A folded-patch antenna with dimensions of 2.5x2.5x1 mm³, operating at 5.7 GHz was analysed considering a 10 kΩ-cm HRPS wafer. The antenna has a –10 dB return loss bandwidth of 50 MHz and an efficiency of 58 %, a performance comparable to glass substrates.

1. Introduction

Wireless multi-hop networks are promoted as a new concept of unobtrusive monitoring and communication [1]. In spite of promising demonstrations made at system level [2], [3], it is still a long way from the presently realized fist-size wireless sensor nodes to the ultimately desired form factor of a few cubic millimeters for such microsystems. Such devices require, first of all, operation at extremely low power levels and thus passive components with very low-losses. The antenna, as the key element in achieving a fully integrated solution, notwithstanding all the development efforts, still remains to be an open challenge. Full integration requires the availability of very-small antennas and effective low-loss materials.

Many of the previously proposed solutions to integrate antennas on-chip have been based on the design of planar antennas using single-crystalline silicon as substrate. The low-ohmic silicon has high losses and then high-resistivity silicon or bulk micromachining is necessary to obtain acceptable antenna efficiency. Nevertheless, the afore-mentioned solutions have the drawback of increased cost, and the micromachining solution have also the penalty of large area used for antenna implementation. In this way, a preferable solution may be to use a combination of a low-loss material with silicon. The new material can be used as antenna substrate and a carrier for any required high-quality factor passives [4], and the silicon will be used to implement the necessary circuitry. Materials will be combined with the use of wafer-level chip-size packaging (WLCSP) techniques, like adhesive wafer bonding and through-wafer electrical via formation, which allows the use of silicon together with different silicon-compatible substrates [5].

An ideal substrate for RF and microwave passives has very high resistivity throughout, a high thermal conductivity, a high dielectric constant and low polarization losses [6]. High-resistivity silicon (HRS) meets most of those requirements but is prone to losses caused by surface channels and is comparably expensive because it is based on sophisticated float-zone crystallization of polysilicon rods. Silicon material with resistivities up to 10 kΩ-cm is made by float-zone processing of undoped polysilicon rods. However, high-resistivity polycrystalline silicon (HRPS) wafers can be obtained from high-resistivity polysilicon rods,

which are normally used for float-zone single-crystalline Si wafers. By avoiding the expensive float-zone crystallization step, the cost of HRPS wafers is significantly reduced, but the favorable material properties are still present. The obtained HRPS substrates have high dielectric constant, low RF loss, high thermal conductivity, perfect thermal matching, and processing similar to single-crystalline silicon. This allows bonding to a core RF silicon wafer which, followed by wafer-to-wafer electrical interconnect formation, enables realization of a variety of novel and complex RF structures (high-Q passives, transmission lines, suspended ground planes, integrated antennas, on-chip shielding, etc.) and represents a truly added value to the concept of wafer-level chip-scale packaging. Moreover, when compared to other solutions, like glass or thick polymer layers (BCB, parylene), higher thermal conductivity and easier processability makes HRPS a better option.

Previously, we have demonstrated that a patch antenna fabricated on a HRPS substrate has performance comparable to one fabricated on glass [5]. In this work, HRPS wafers are proposed as low-loss substrates for three-dimensional integration of folded-patch antennas based on wafer-level chip-scale packaging fabrication techniques.

2. Antenna design

Aiming for small dimension devices, a small antenna design is a key factor. The effectiveness of HRPS to integrated complex antenna designs was tested with a folded-shorted patch antenna, as shown in Fig. 1.

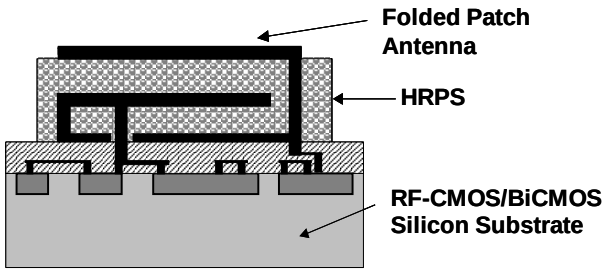
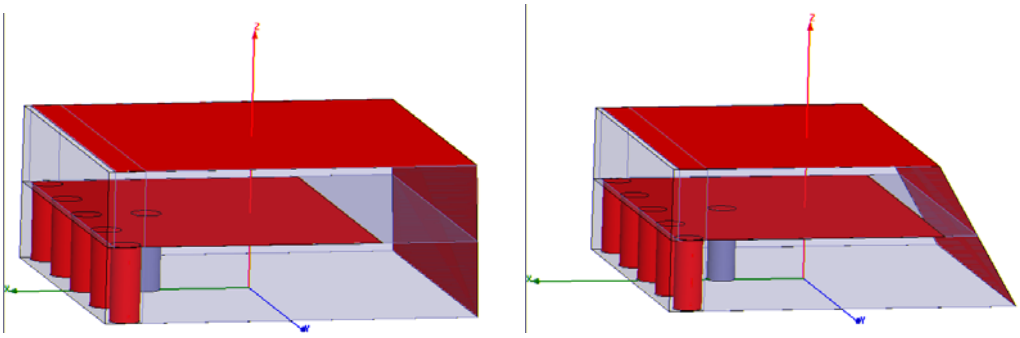


Fig. 1: Concept of a folded-patch chip-size antenna integrated using WLCSP fabrication techniques.

It consists of three horizontal metal sheets that are electrically connected by two vertical metal walls. All this is embedded in a dielectric substrate having certain electrical permittivity and dielectric losses. These two parameters together with the antenna geometry and its actual dimensions will determine its radiation characteristics and overall performance. For good performance, the metallization layers should have very low resistivity and the substrate should have the lowest losses possible. To obtain an antenna with small dimensions, a material with high electrical permittivity is also desirable.

2.1 Modeling

The antenna model was built using the high-frequency structure simulator (HFSS) from Ansoft. This simulator was already used to design folded-patch antennas on glass, as well double-folded patch antennas on a Rogers substrate. The material properties used in the simulations were first obtained from a test wafer [8]. The proposed, on-chip integrated, folded short-patch antenna models are shown in Fig. 2. In the first model, the connection between the ground plane and the top patch is assumed to be a vertical wall. In the second one, it as a slanted wall. This is a better option from the fabrication point-of-view.



a) b)

Fig. 2. Model for the proposed shorted-folded patch antenna: a) with vertical wall, b) with slanted wall.

The antenna was designed inside a box of 2.5x2.5x1 mm^3. The via-fence, as well the feeding point, is modeled as being metallized holes with diameter of 200 μm of. The length of the middle patch was chosen to provide an antenna operating at frequency of 5.7 GHz. This is a frequency inside the 5-6 GHz ISM band. The feeding point position was adjusted to obtain good impedance match to 50 Ω. The slanted wall was considered to make an angle of 30º with the vertical. The antenna feeding was made through a coaxial cable connected to de feeding point.

2.2 Fabrication

The major steps for the fabrication of this device require the formation of trough-wafer vias, via metallization, metal deposition, patterning, and wafer bonding. We have previously demonstrated such fabrication sequence using glass substrates [7] where via formation is more difficult.

Since standard and well-known processing techniques for silicon wafers, as well WLSCP techniques, can be used to process the HRPS wafers, the fabrication of this device does not present major problems. Care has to be taken with metallization within the through-substrate vias and on the vertical sidewalls to achieve sufficient metal layer thickness.

3. Results and discussion

The models built were used to obtain the expected performance for two different wafer resistivities: 4 kΩ-cm and 10 kΩ-cm, and two different geometries: vertical and slanted wall. In Fig. 3-a, the return loss plot is displayed for a design with a 4 kΩ-cm wafer and a slanted wall. Fig. 3-b shows the radiation diagram for the same design.

The obtained bandwidth at –10 dB return loss was ~40 MHz with an efficiency of 31%. Instead, if the structure with the vertical wall is used, it is possible to increase the efficiency to 38%, and the bandwidth rises to ~50 MHz. If a 10 kΩ-cm wafer is considered, the antenna with the slanted wall has a bandwidth of 25 MHz and efficiency of 48 %. The antenna with the vertical wall allows a bandwidth of ~30 MHz and an efficiency of 58%. These values are very similar to what is obtained with glass substrates [7].

It was observed that the antenna dimensions, as well substrate losses, strongly affects the efficiency and bandwidth. For a 5.7 GHz operation frequency, an antenna size of 3x3x1 mm^3 is expected to be necessary for a –10 dB return loss bandwidth of 50 MHz with efficiency above 50%.

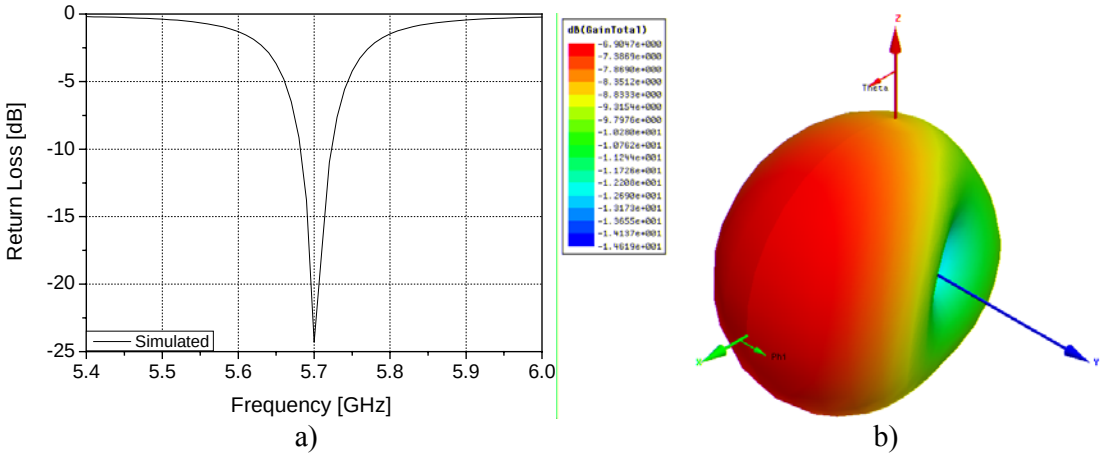


Fig. 3. Results for an antenna designed on a 4 kΩ-cm wafer with a slanted wall: a) return loss versus frequency used to obtain the operating frequency and bandwidth, b) radiation diagram at 5.7 GHz.

4. Conclusions

The use of HRPS substrates makes on-chip antenna integration possible with an antenna efficiency and electrical performance similar to the one obtained with glass. Due to a higher dielectric constant, integration on HRPS results in a reduced antenna size: 12.4x11.7 vs. 7.7x7.6 mm^2 for a patch antenna and 4x4 vs. 3x3 mm^2 for folded-patch antenna at 5.7 GHz. Next to that, the inherent problems associated with glass substrate processing (e.g. difficulty to form high-aspect ratio vias) are avoided.

Acknowledgement

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