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Sensors and Actuators A 125 (2006) 217–222
SENSORS AND ACTUATORS A PHYSICAL
www.elsevier.com/locate/sna

Integrated chip-size antennas for wireless microsystems: Fabrication and design considerations

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Received 3 June 2004; received in revised form 12 July 2005; accepted 24 July 2005
Available online 22 September 2005

Abstract

This paper reports on fabrication and design considerations of an integrated folded shorted-patch chip-size antenna for applications in short-range wireless microsystems and operating inside the 5–6 GHz ISM band. Antenna fabrication is based on wafer-level chip-scale packaging (WLCSP) techniques and consists of two adhesively bonded glass wafers with patterned metallization and through-wafer electrical interconnects. Via formation in glass substrates is identified as the key fabrication step. Various options for via formation are compared and from these, a 193 nm excimer laser ablation is selected for fabrication of the antenna demonstrator. The fabricated antenna has dimensions of 4 mm × 4 mm × 1 mm, measured operating frequency of 5.05 GHz with a bandwidth of ∼200 MHz at the return loss of −10 dB and a simulated radiation efficiency of 60% were achieved.

Keywords: Chip-size antenna; Wafer-level packaging; Wireless microsystem; Excimer laser ablation; Via fabrication

1. Introduction

Application of distributed systems equipped with short-range wireless communication capabilities will highly be facilitated if cheap and easy-to-use ‘on-chip’ or ‘in-package’ solutions would be available. On-chip integrated transceivers, from baseband to antenna input/output, have already become technologically possible. However, an on-chip antenna, as the key element in achieving a fully integrated solution, is still an open challenge. The characteristic antenna dimensions are proportional to the operating wavelength. Migration of short-range wireless communication systems to higher frequency bands like the 5–6 GHz ISM band allows smaller antennas and thus facilitates their on-chip integration.

Several small and planar antenna types have been proposed for wireless communications [1] but none of them was designed to meet all the restrictions and requirements set by on-chip integration. These include the properties of available substrates and restrictions imposed by processing technologies. Using of a patch-type antenna and silicon (dielectric constant of ∼12) as the antenna substrate will be a straightforward solution for on-chip antenna integration. However, since the ‘standard’ silicon is a lossy material, high-resistivity silicon or bulk micromachining have to be used in order to decrease dielectric losses and thus providing antenna having reasonable efficiency. A different approach is to use an additional spacer substrate having low dielectric loss that can be stacked on top of an active silicon wafer and that can be processed using a conventional IC fabrication technology. Glass substrates having moderate dielectric constant, low dielectric losses and their availability with composition having thermal coefficient of expansion matched to silicon, are an interesting candidate [2].

Introducing of a new material is not inevitably a complication. Wafer-level packaging (WLP) techniques, based on MEMS technology, when applied to packaging of RF silicon ICs represent truly added value as at a limited cost 3D passive structures can be realized. Application of adhesive wafer bonding and through-wafer electrical via formation, allows stacking of different substrates together with silicon [3]. The use of glass wafers reduces the losses, but since typical glass substrates have dielectric constant in the range of 4–6.5, patch-type antennas would be rather large. The antenna dimensions can however be reduced

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doi:10.1016/j.sna.2005.07.016

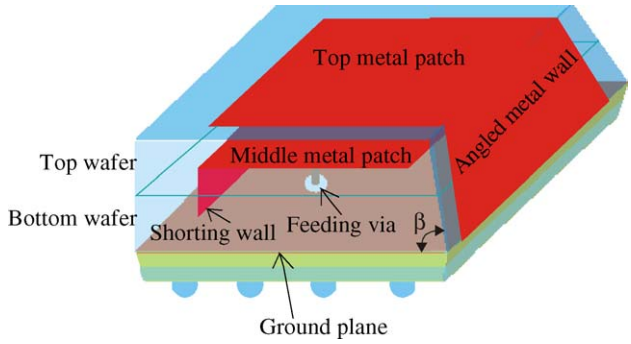

Fig. 1. Concept of the proposed folded shorted-patch antenna.

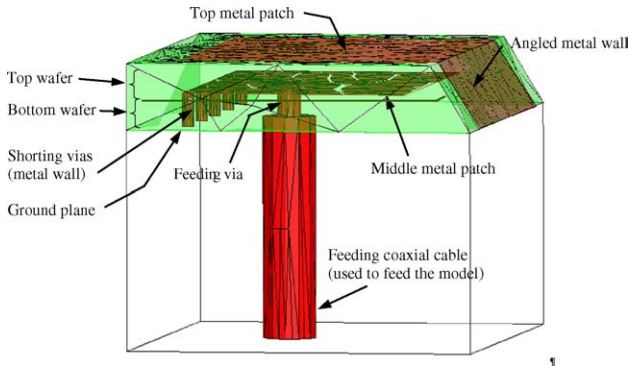

Fig. 2. HFSS model of the folded shorted-patch antenna used for electrical analysis.

using an advanced antenna design like folded or shorted structure [1]. In this way, application of glass substrates enables a small on-chip antenna and RF electronics direct coupling. This offers potential of low cost, low form factor and simplified assembly.

A folded shorted-patch antenna (FSPA) can be used as a compact solution for the on-chip antenna integration [4]. Due to its rather complicated structure, its implementation is not trivial. We have adapted the WLP technology of Shellcase [5] for on-chip integration of such folded-patch antenna. The envisioned application and the fabrication constraints define some critical antenna parameters that have to be investigated. In this paper, design and process considerations for on-chip implementation of an FSPA are presented.

2. Antenna design

The proposed, on-chip integrated, folded short-patch antenna is shown in Fig. 1. It consists of three horizontal metal sheets that are electrically connected by two vertical metal walls. All this is embedded in a dielectric substrate having certain electrical permittivity and dielectric losses. These two parameters together with the antenna geometry and its actual dimensions will determine its radiation characteristics and overall performance.

For the best performance, the metal sheets should have minimum resistivity and the dielectric should be a low-loss material, which allows high efficiency. Also, to achieve small antenna dimensions, a substrate with high electrical permittivity is desirable. High antenna efficiency requires thicker substrates (>300 μm) and therefore high aspect ratio vias in glass are required.

At frequencies above 1 GHz, glass becomes a very attractive option. Its main advantages are low losses, reasonable ε_r, availability in a form of wafers with any required thickness and diameter, and last but not least low cost. There is also sufficient experience in processing of glass wafers from MEMS and WLP applications [3].

The antenna was designed to operate at 5.1 GHz, a frequency chosen to be inside the 5–6 GHz ISM band. All the simulation analysis was performed with an antenna model that was built using the High Frequency Structure Simulator (HFSS 8.5) from Ansoft, a 3D tool based on finite element modeling. This simulation tool was intensively used previously in our patch antenna design [2,6], where good match between modeling and experimental results was achieved. The complete model design requires the knowledge of the glass wafer properties used to fabricate the prototype. These electrical characteristics were obtained using the method described in [7]. The developed antenna model is displayed in Fig. 2.

Fig. 3 shows return loss of the proposed FSPA. It was considered the use of two stacked, 500 μm thick, Corning Pyrex #7740 glass substrates and the antenna was designed with the overall dimensions of 4 mm × 4 mm × 1 mm. The metallization layers used in simulations were aluminium with 2 μm of thickness, except for via metallization were it was considered a thickness of 0.1 μm. Then, a simulated radiation efficiency of 60% and a bandwidth of ∼150 MHz at −10 dB return loss have been predicted. The predicted far-field radiation diagrams (Fig. 4) shows that the power is being mainly radiated upwards and the antenna interference with backside devices is minimized.

From the fabrication point of view, it is preferable to keep the overall antenna thickness small. To achieve this, thin or thinned wafers can be used. However, the wafer thickness is a relevant parameter that influences the antenna performance, since it corresponds to the antenna substrate thickness. To study this effect, all the FSPA dimensions were kept constant, except the wafer

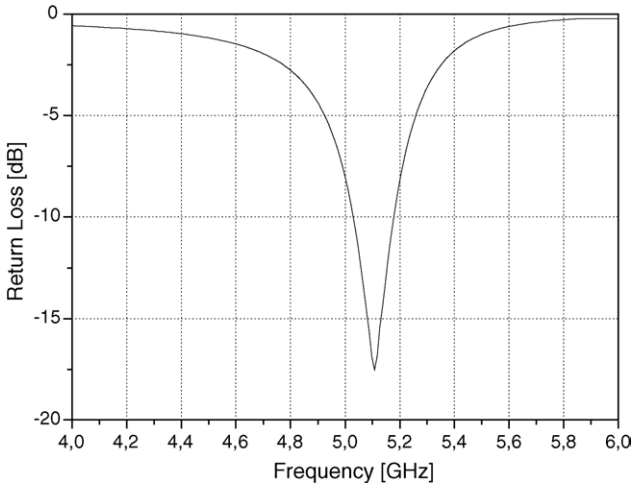

Fig. 3. Simulated return loss of the projected folded shorted-patch antenna with #7740 glass substrate.

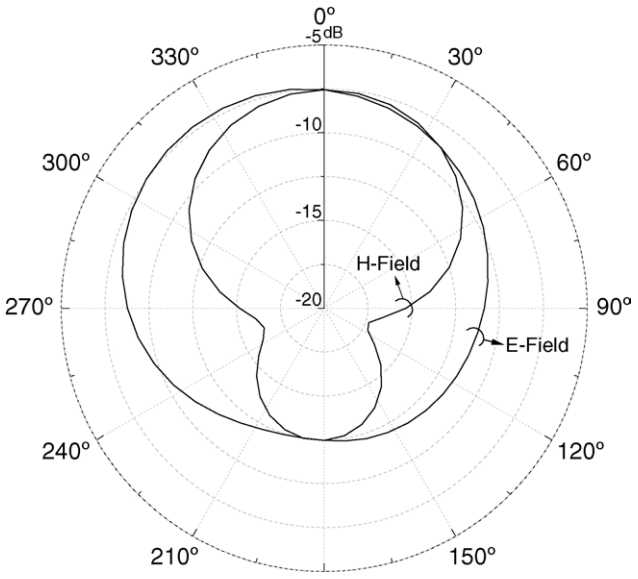

Fig. 4. Simulated co-polar far-field gain patterns of the projected folded shorted-patch antenna ($\beta = 65^\circ$, see Fig. 1).

thickness, h, which was as a parameter. The obtained results for the return loss are presented in Fig. 5. It can be observed that decreasing the wafer thickness from 500 μm down to 100 μm leads to a reduction of the antenna operating frequency. This is a desirable effect since, for the same operating frequency, the antenna can be smaller. However, as the results in Fig. 5 shows, a thinner substrate and thus a smaller volume of the antenna dielectric will cause reduction of the antenna radiation efficiency as well as reduction of the antenna bandwidth. If the wafer thickness is increased to 800 μm, instead of a monotonous increase with thickness increment, the operating frequency decreases again. This contradiction requires further explanation. Logical expectation is that with increasing the wafer thickness and thus larger antenna electrical length, the antenna operating frequency will decrease. This is what actually happens for wafer thickness above 500 μm. However, in this particular design, the length of the middle patch is kept constant and therefore the gap between the middle patch and the slanted ground plane will vary significantly when the wafer thickness is modified. For wafer thickness below 500 μm, the variation in this gap width becomes the dominating effect in setting the operating frequency [8]. When the wafer thickness decreases, the gap width increases and the antenna operating frequency is decreased. Table 1 summarizes the observed effects when the wafer thickness was changed, where efficiency means antenna radiation efficiency.

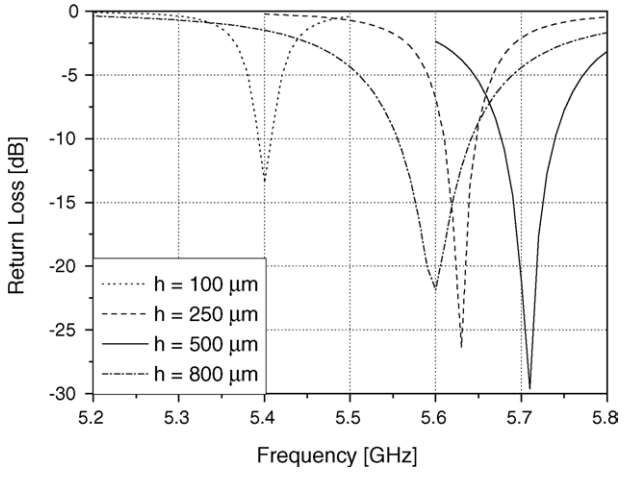

Fig. 5. Return loss of the FSPA for different substrate thickness values.

Table 1
Overview of selected antenna properties for different substrate thickness values

Substrate thickness (μm)	Frequency (GHz)	Bandwidth (MHz)	Efficiency (%)
100	5.4	17	23
250	5.63	39	48
500	5.71	62	66
800	5.6	88	76

3. Fabrication

3.1. Via fabrication

The most demanding fabrication step required to realize the proposed antenna structure, is the through-wafer high-aspect-ratio via forming in glass. There are various techniques that can be used for via fabrication in thick glass substrates (>300 μm), but all of them have severe limitations in their throughput or achievable aspect ratios [3,9]. We have explored two of them: powder blasting and laser ablation.

Powder blasting is a widely used method in glass processing. Its main disadvantage is that the typical side-wall slope is about 75° which results in rather limited achievable aspect ratio of powder-blasted vias of ∼2.5:1. Higher aspect ratios are possible by performing the sand blasting from both wafer sides. Other disadvantage is rather high surface roughness of the sand-blasted vias. The main advantage is its sufficiently high throughput, which makes this technique suitable for industrial applications.

Laser ablation is a popular technique for via fabrication in electronic packaging. However, the application of commonly used lasers with infrared or visible light sources is not possible due to the high transparency of glass in this wavelength region. We have tested a third harmonic Nd:YAG laser (wavelength 355 nm), KrF (248 nm) and ArF (193 nm) excimer lasers. The results achieved for the 355 and 248 nm light sources were not satisfactory due to the insufficient beam absorption and forming of local cracks.

Application of a 193 nm laser gives very good results as shown in Fig. 6. Due to the nature of the gas-based excimer lasers, their spatial coherence is low and therefore beam focusing into a small spot is much more difficult in comparison to the UV solid state lasers. Therefore, direct ablation of required patterns was not possible and a projection mask with a 30:1 reduction optics was used. Fig. 6 shows microphotographs of 200 μm diameter vias and a 100 μm wide rectangular slot formed in a 500 μm thick glass wafer using a 193 nm excimer laser. The ablation process causes surface contamination due to the deposi-

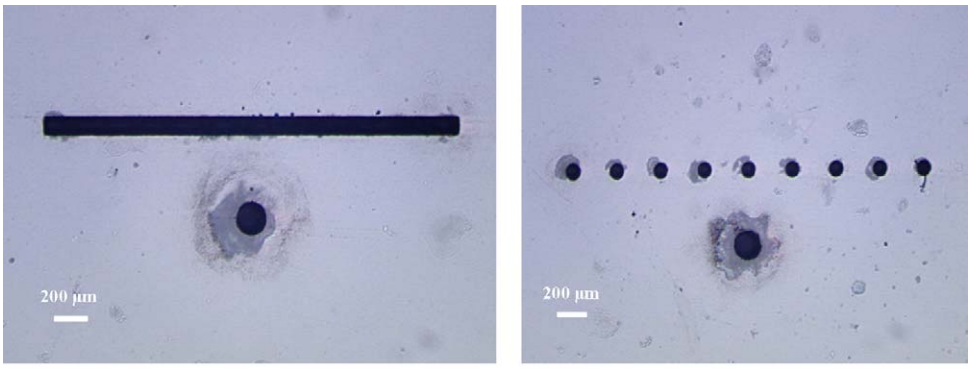

Fig. 6. Microphotograph of a 500 μm thick AF-45 glass substrate with laser ablated through-wafer vias. The antenna patch-to-ground connection is realised using (a) a 100 μm × 3000 μm slit; (b) an array of 9 μm × 100 μm vias. Note that the photos are taken from the wafer back side.

tion of ablated particles in the close vicinity of ablated vias. This can be easily avoided by spinning on a protective water-soluble polyvinyl alcohol (PVA) layer before the ablation step and its subsequent removal after the ablation was completed. Note that no protection layer has been applied on samples in Fig. 6 and therefore contamination on the wafer surface resulting from the ablation process is clearly visible.

The main disadvantage of using an excimer laser ablation for via formation in glass is its very low throughput which is depending on the to-be-etched pattern and glass thickness and might reach hours per wafer. This could be significantly improved by application of UV solid state lasers (e.g., high harmonic Nd:YAG with 266 or 213 nm) where due to their high spatial coherency direct ablation with a highly focused beam is possible. Nevertheless, the 193 nm excimer laser gives very good results and is suitable for prototype fabrication.

3.2. Fabrication sequence

The schematic fabrication sequence is presented in Fig. 7. The starting material is a 100 mm diameter, 500 μm thick AF-45 glass substrate in which arrays of high-aspect-ratio circular vias (diameter of 100 and 200 μm) or rectangular slots (100 μm × 3000 μm) were formed using a 193 nm excimer laser ablation through a projection mask and a 30:1 reduction optics. The slight contamination of the wafer surface due to the ablation process could be avoided by application of a protective PVA layer that is removed after via ablation.

After the via formation, a 4 μm thick Al layer have been sputtered from both wafer sides and patterned using electroplated photoresist on the wafer front side defining the middle antenna patch. This simple approach based on double-side sputtering of relatively thick Al layer is sufficient for demonstration purposes, but yields especially for high-aspect ratio vias (>3:1) rather thin metal layer in the middle of the vias. This will inevitably cause increased RF losses and decrease antenna efficiency. Better option is to sputter a Ti:Cu seed layer and perform additive electroplating of thick Cu layer with subsequent removal of the seed layer [9].

The fabrication sequence continues by glass-to-glass adhesive bonding to the upper glass substrate using BCB as adhesive [9]. The wafer stack is then temporarily attached to a supporting foil commonly used in wafer dicing. In two dicing steps a V-groove trenching is performed. During the first dicing step a standard thermocarbon blade is used to dice a rectangular pre-alignment trench. In the second dicing step this pre-alignment trench is shaped using a V-shaped thermocarbon dicing blade into its final form. Accuracy in the micrometer range can be achieved. At this stage the wafer stack disintegrates into strips that are detached from the supporting foil and subsequently individually processed. After cleaning of the individual strips, a 2 μm thick Al layer is sputtered to form the upper antenna patch. The processing sequence is completed by singulation into individual dies by standard dicing, which also defines the lateral antenna dimensions.

4. Results and measurements

A prototype was fabricated with the technique described in Fig. 7, where the laser ablation was used to obtain the through-wafer vias. A photo of the prototype is shown in Fig. 8. To measure the fabricated antenna, it was necessary to attach it to a PCB board, where a 50 Ω microstrip line was designed to interface the antenna with a coaxial connector that provides the connection to the vector network analyser. The connection between the microstrip line and the antenna feeding via was made by wire bonding. The return loss measurements were performed with an E8358A vector network analyser. Fig. 9 shows the measured and simulated values for the fabricated prototype. The difference between the projected and measured bandwidth are mainly due to the thickness of the metal inside the shorting and feeding vias, as we were able to verify by simulation. If the metal thickness of vias metallization changes from, e.g., 2 to 0.02 μm it was obtained by simulation that the bandwidth changes from ∼50 to ∼200 MHz. The small shift in the operating frequency from 5.1 to 5.05 GHz is due to a small increase in the dimensions of the top metal patch. This top metal patch was first designed to be defined by patterning but to reduce costs, was defined by the singulation step (Fig. 7), resulting in a larger patch.

The simulated values on Fig. 9 were obtained after antenna fabrication, where relevant process dependent parameters were

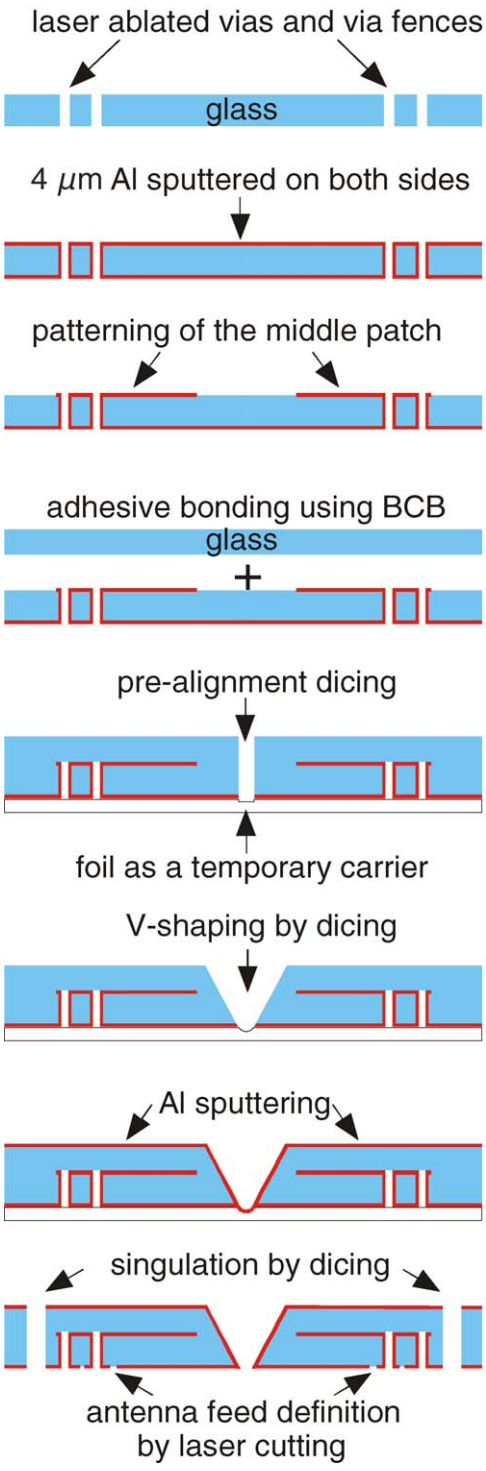

Fig. 7. Schematic fabrication sequence using laser ablated vias.

updated to better match the values obtained during antenna processing. Also, it was included the effect of the ground plane that was used to mount the antenna for simulations. After that adjustment, it was possible to obtain a good agreement between de measured and the simulated data. The final antenna dimensions are 4 mm × 4 mm × 1 mm, the operating frequency is 5.05 GHz with a bandwidth of ∼200 MHz.

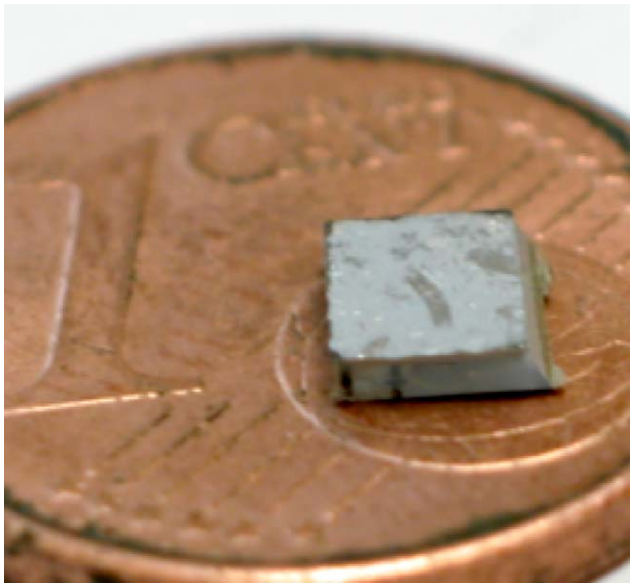

Fig. 8. Photo of the antenna prototype.

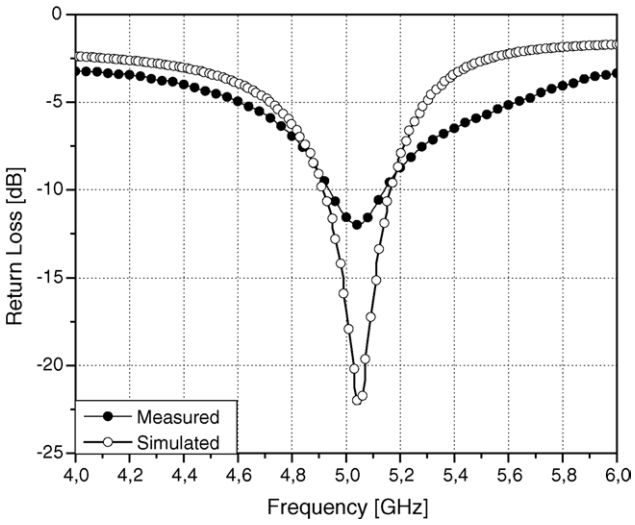

Fig. 9. Measured and simulated return loss of the fabricated antenna prototype.

5. Conclusions

In this work, we have demonstrated that fabrication of folded shorted-patch antennas operating at 5–6 GHz is feasible using WLP techniques and that their performance make them suitable for microsystems aiming at wireless short-range links. We have proposed and investigated fabrication options for realization of an on-chip integrated FSPA based on WLP techniques. Various via fabrication techniques in glass substrates, as the critical step in fabrication sequence, have been compared and a 193 nm excimer ablation laser was selected as the most suitable for the antenna prototype.

The fabrication sequence is thus based on an excimer laser drilling of high-aspect-ratio vias in glass with subsequent sputtering and patterning of the bottom and middle metal layers. This is followed by glass-to-glass adhesive bonding, V-groove dicing, upper metal layer sputtering. Final dicing into individual

chips defines the lateral antenna dimensions. Measurement data obtained from the fabricated prototype were used to update the initial simulation parameters enhancing the design system for validation of future antenna models.

A chip-size folded shorted-patch antenna fabricated using WLP techniques was designed, fabricated, and characterized. This folded antenna has smaller dimensions (4 mm × 4 mm × 1 mm) when compared to the previous works [10,11]. It operates at 5.05 GHz, a frequency inside the 5–6 GHz ISM band, and with a bandwidth of ∼200 MHz, which is sufficient for applications in wireless sensor networks.

Acknowledgements

The authors would like to thanks the Portuguese Foundation for Science and Technology (FEDER, POCTI/ESE/38468/2001 and SFRH/BD/4717/2001) and EU (project Blue Whale IST-2000-30006) for funding this work.

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Biographies

Paulo M. Mendes graduated in 1995 and received his MSc degree 1999, both in electrical engineering from the University of Coimbra, Coimbra, Portugal. From 1997 to 1999, he was a lecturer at the Polytechnic Institute of Castelo Branco, Portugal. Since 1999, he has been a lecturer at the Department of Industrial Electronics, University of Minho, Portugal. He is currently working towards his PhD degree in Industrial Electronics and is involved in the research on wafer-level chip-scale packaging for RF applications.

Alexander Polyakov received the BS and MSc degree from St. Petergsburg state Technical University, Russia both in physics. In the end of 2000, he started his PhD studies at Laboratory of Electronic Components, Technology and Materials (ECTM) at Delft University of Technology. His main research areas are wafer-level chip-scale packaging, on-chip electromagnetic isolation and reliability.

Marian Bartek received his MSc degree in microelectronics and optoelectronics from the Slovak Technical University, Bratislava, Slovakia in 1988 and a PhD degree in electrical engineering at the Delft University of Technology, The Netherlands in 1995. From 1996 to 1999, he was a post-doctoral fellow in the Electronic Instrumentation Laboratory, Delft University of Technology, dealing with research on technological aspects of integrated silicon sensor systems. Presently, he is with the Laboratory of High-Frequency Technology and Components (HiTeC), Delft University of Technology, as an assistant professor, working in the area of microsystem interfacing and wafer-level packaging for RF applications.

Joachim N. Burghartz received the MSc (Dipl. Ing.) degree from the RWTH Aachen, Germany, in 1982 and the PhD (Dr. -Ing.) degree from the University of Stuttgart, Germany, in 1987, both in electrical engineering. From 1982 to 1987, he was with the University of Stuttgart, Germany, where he developed sensors with integrated signal conversion with a special focus on magnetic-field sensors. From 1987 to 1998, he has been with the IBM Thomas J. Watson Research Center in Yorktown Heights, New York. His earlier research work at IBM included device applications of selective epitaxial growth of silicon, Si and SiGe high-speed transistor design and integration processes, and deep-submicrometer CMOS technology. For the past few years, he has been engaged in the development of circuit building blocks for SiGe RF front-ends, with a special interest in the integration of high-quality passive components on silicon, which also included micromachining techniques. He is now a chairman of the Laboratory of High-Frequency Technology and Components (HiTeC) with an interest in silicon RF technology, ranging from investigations on materials to RF circuit building blocks. He is also the scientific director of the Delft Institute of Microelectronics and Submicrontechnology (DIMES). Dr. Burghartz is an IEEE Fellow and an IEEE Distinguished Lecturer.

Jose Higino Correia graduated in physical engineering from University of Coimbra, Portugal in 1990. He obtained in 1999 a PhD degree at the Laboratory for Electronic Instrumentation, Delft University of Technology, working in the field of microsystems for optical spectral analysis. Presently, he is an associate professor in Department of Industrial Electronics, University of Minho, Portugal. His professional interests are in micromachining and microfabrication technology for mixed-mode systems; solid-state integrated sensors, microactuators and microsystems.