A 4.2 mW 5.7-GHz frequency synthesizer with dynamic-logic (TSPC) frequency divider

J. P. Carmo, P. M. Mendes, J. H. Correia
University of Minho, Dept. Industrial Electronics
Campus Azurem, 4800-058 Guimaraes, PORTUGAL, **jcarmo@dei.uminho.pt**

***Abstract* - This paper presents a Phase-Locked Loop (PLL) used as a frequency synthesizer for a radio-frequency (RF) transceiver for use in the 5.7 ISM band, which were designed in the UMC RF 0.18 µm CMOS process. The PLL produces a set of different 16 digitally programmable frequencies in the [5424; 5830 MHz] frequency range. The low-power operation is achieved with the use of dynamic logic in the feedback path. Simulations shown a total power consumption of 4.2 mW. Target applications are wireless sensors and microsystems applications that need RF transceivers for operation in the 5.7 GHz band.**

***Keywords* - Frequency synthesizer, CMOS, low-power design, high-speed digital circuits.**

I. INTRODUCTION

CMOS technology has reached its maturity. Therefore, design engineers used it for developing radio-frequency (RF) circuits. The advantages of CMOS technology are the higher integration, low-power consumption, low-voltage supply and low-cost compared with Bipolar technology. The use of CMOS process with low length for the channels of the MOSFETs is very important for high-frequency devices. The UMC RF 0.18 µm CMOS process allows to trade the high-frequency capability of minimum-length transistors with lower current consumption by biasing the devices at lower current densities, even for devices working at RF. This process provides a poly and six metal layers, the use of integrated spiral inductors (with a quality factor of 10), high-resistor values (a special layer is available) and a low power supply of 1.8 V.

This paper presents a low-power/low-voltage frequency synthesizer as a constitutive block of a RF transceiver for use in the 5.7 GHz ISM band.

II. ARCHITECTURE OF THE PLL

The synthesizer is a Phase-locked Loop (PLL) with a integer divider in the feedback loop, whose dividing ratio is digitally programmed in order to produce an output in the [5424; 5830 MHz] frequency range. Figure 1 shows the block diagram of the PLL described in this paper. This the PLL has a reference generator circuit with a crystal based oscillator at 13.56 MHz, followed by a Phase-Frequency Difference Circuit (PFD), a current steering charge pump (CP), a third order passive filter. The passive section output is connected to the VCO, that generates the desired frequency range of [5424; 5830 MHz]. Finally, in order to get the desired frequency in the previous range, this one must be divided by 400+2*S*, where *S* is integer and belongs to the interval {0,1,…15}. Then the output of the divider is connected to the PFD, closing the loop. The output frequency produced by the PLL depends from the divider ratio, *N*, and is $f_{out}=f_{ref}.N$ [Hs]. The PLL acts a frequency multiplier of the reference frequency, f_{ref} [Hz].

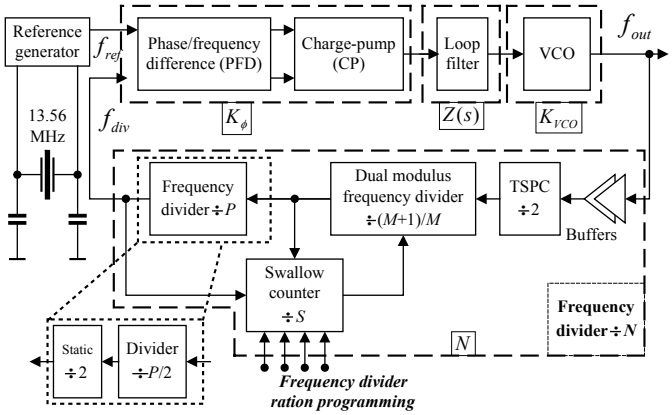


Figure 1: The block diagram of the PLL.

In a RF transceiver, the frequency synthesizer is one of the most challenging blocks of RF transceivers, because it operates with the highest speed and the stringent trade-off between the speed and the power consumption. Typically, the blocks with the biggest power consumptions include the Voltage Controlled Oscillator (VCO), the frequency divider and the buffers. Thus, the efforts to reduce the power consumption and increase the speed, must always take place in the design.

A. Voltage-controlled oscillator (VCO)

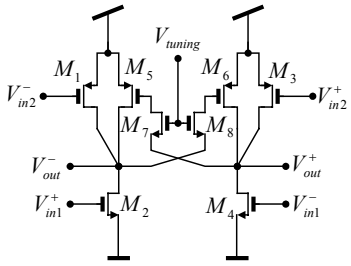
It was chosen a ring-type VCO instead of a tuned LC VCO, in order to save on-chip area. Ring oscillators have more phase noise than LC oscillators [1]. For overcoming this limitation, the bandwidth of the PLL must be high enough to "clean-up" the output spectrum around the 5.7 GHz interval [2].

The ring oscillators are classified according theirs switching characteristics, e.g., non-saturated and saturated types [3]. For the non-saturated VCOs, the phase-noise is:

$$N = \frac{4kR\Delta T}{1+(2\pi f_m RC)^2} \qquad (1)$$

where ΔT [s] is the on-time of the transistors inside a delay cell, f_m [Hz] is the offset frequency from the carrier, and RC [s] is the equivalent time-constant which is taken from the first-order model of the delay cell. An analysis to the equation (1), reveals that a short on-time is desired to have a low noise power. In order to such a goal be achieved, a simple inverter-based ring oscillator is not suitable, because a full switching never happens, thus a certain kind of anticipation in order to force a full switching must be done. Figure 2(a) shows an unitary cell of a ring oscillator, which is of differential type and have two cross-connections (M_5/M_7 and M_6/M_8) between its inverter cells (M_1/M_4 and M_2/M_3) in order to make a latch to force the inverters to fully saturate [3]. The complete VCO uses a set of five inverter cells, which were connected as shown in Figure 2(b).

a)



MOSFET	W [μm]	L [μm]
M_1	1	0.18
M_2	6.5	0.18
M_3	1	0.18
M_4	6.5	0.40
M_5	9	0.40
M_6	9	0.18
M_7	0.6	0.18
M_8	0.6	0.18

b)

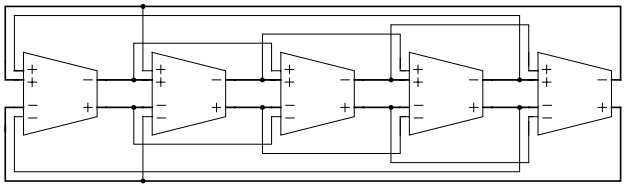


Figure 2: Voltage-control oscillator: a) saturated unity cell, with the MOSFET's dimensions and b) the complete VCO with five inverter cells.

B. PFD-CP

The reference frequency, f_{ref} [Hz] was chosen to be 13.56 GHz, thus, the speed constraints for the phase/frequency difference circuit (PFD) and for the charge-pump (CP) are not of special concern, thus conventional structures can be used without the risk to have an unpredictable high power consumption [4].

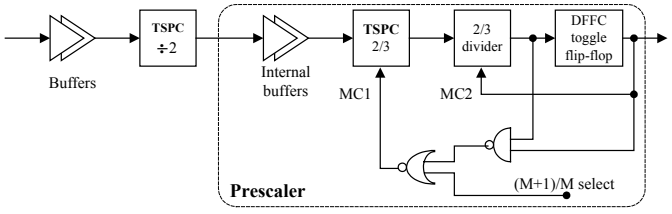
C. Frequency divider

Perhaps, this is the most complex and challenging stage in a PLL, which must be designed with very care in order to keep the power at a low acceptable level, at the same time it meets the speed specifications. In high frequency PLLs, the high power consumption is mainly due to the first stages of the frequency divider that often dissipates half of the total power. The use of conventional static CMOS logic in the first stage is not possible. This is due to the high input frequency [5]. The overall divider has two true-single-phase-clock (TSPC) frequency dividers, that halves the following dividers, which use static logic.

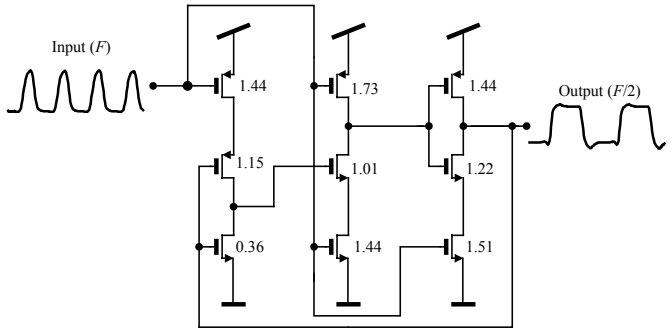
As depicted in Figure 1, the desired divider ratio in the feedback path is N=2($M.P$+S), where (M+1)/M (with M=10) are the variable frequency divider ratios of the prescaler, S=20 is the divider ratio of the main counter, and S is the divider ratio of the swallow counter. The main counter has a divider by P/2=10 followed by a toggle flip-flop, which makes the feedback signal at the divided input, f_{div}, of the PFD to have a duty-cycle of 50% (as it happens with the reference signal at the main input, f_{ref}, of the PFD). Compared with other situations, where the PFD's inputs have different duty-cycles, this minimises possible delays that can arise, during the locking process of the PLL. This is of special concern in situations when the PLL is turned on or after an order to switch the frequency at its output.

Figure 3(a) shows the structure of the TSPC frequency divider by two and prescaler. The frequency at the input of the prescaler is in the range [2712; 2915 MHz], and previous measurements shown for this technology that for frequencies above 2 GHz, it exists an impossibility to make frequency division with the use of static logic. Thus, TSPC logic must be used in order to make work the further circuits in static logic.

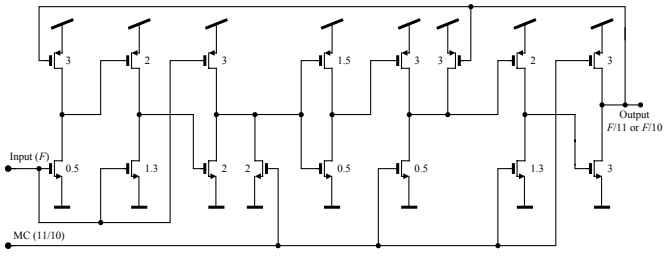
The TSPC logic was used again to overcome the impossibility to implement the first stage of the prescaler (the frequency divider by 2/3 with modulus control) with static logic in this technology. However, in order to the TSPC dividers work properly, the inputs must be rail-to-rail. The length of all MOSFETs is equal to the minimum allowed for this technology, e.g., 0.18 μm, so the illustrated values in Figures 3(b) and (c) are the widths, [μm], of MOSFETs.



a)



b)



c)

Figure 3: a) The block diagram of the TSPC divider by two, followed by the prescaler; b) the schematic of TSPC divider by two; and (c) the schematic of the prescaler. The buffers are not shown in the schematics.

In the global structure of the frequency divider, the swallow counter plays an important role, e.g., the fixed division by 10 or 11 is extremely easy to achieve. The difficulty is to

establish the precise intervals in which the division must be made and why. Figure 4 shows three situations of divisions give by 200=(15×10)+5×10, 203=(3×11+12×10)+5×10 and 215=(15×11)+5×10 (for the global divisions of 400, 406 and 430), as well as the behaviour of the $(M+1)/M$ control signal to the prescaler. The CLK signal is the signal at the output of the VCO, VCOout, after to be divided by two in the TSPC frequency divider, thus, this is why half of the countings are refereed and not the exact value.

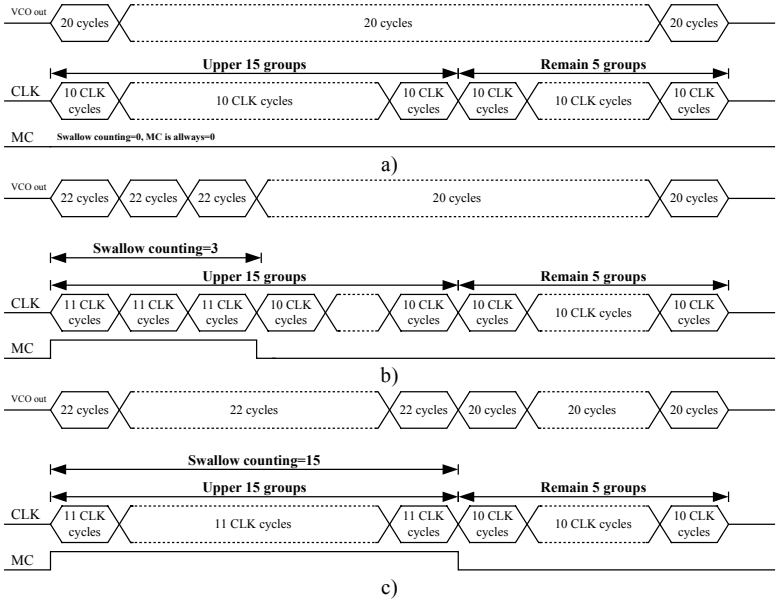


Figure 4: Swallow counting process to generate the appropriate MC signal for the prescaler, for three global division ratios: a) 400, b) 406 and 430.

Basically, the idea behind the frequency division is the definition of a general rule to simultaneously make the division of the minimum to the maximum in steps of one (in this case, from 200 to 215), and further in steps of two. In this case, the difference between the two limits is 30 and the swallow counting is from 0 to 15, so the values $11\times S+10\times[\max(S)-S]+50$, with $S\in\{0,1,\ldots,15\}$ and $\max(S)=15$ will be a useful solution to the problem. Then the final division ratios in steps of two, are ensured by the first TSPC toggle flip-flop, at the same time the last static toggle flip-flop in the main counter, P, ensures that the divided signal has a duty-cycle of 50%. To finish, the swallow counter is essentially a descendent programmable counter and it operates as follows: the counter is initiated to the desired value S, and then it starts to counting in the descending order until zero. Meanwhile, the MC signal is activated, then it falls down, except in the case the counting S is already initialised at zero.

A. Loop-filter

As it was said before, the ring oscillators have more phase noise than *LC* oscillators [6] thus, a third order passive filter, composed by a second order section (C_1, C_2 and R_2) and a first order section (C_3 and R_3), providing an additional pole it is used. The first order filter reduces spurs caused by the multiples of reference frequency, whose consequence is the increasing of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL bandwidth and below the reference. The stability in the loop is obtained with a phase margin of $\pi/4$ rad or higher. The chose of passive components must obey to the following: given the bandwidth, f_p [Hz], the phase margin ϕ_p [rad], the minimum attenuation, A_{min} [dB], measured at multiples of the spurious reference frequency, f_{ref} [Hz], which is imposed by the low-pass filter R_3C_3, it will result in the five passive components of the loop-filter [7]:

$$C_1 = \frac{\tau_1}{\tau_2}\times\frac{K_\phi K_{VCO}}{(2\pi f_p)^2 N}\times \times\sqrt{\frac{1+(2\pi f_p)^2\tau_2^2}{[1+(2\pi f_p)^2\tau_1^2]\times[1+(2\pi f_p)^2\tau_3^2]}} \quad (1)$$

$$C_2 = C_1\left(\frac{\tau_2}{\tau_1}-1\right) \quad (2)$$

$$R_2 = \frac{\tau_2}{C_2} \quad (3)$$

where the time constants τ_1, τ_3 and τ_2 are respectively

$$\tau_2 = \frac{(2\pi f_c)^{-2}}{\tau_1+\tau_3} \quad (4)$$

$$\tau_3 = \frac{\sqrt{10^{\frac{A_{\min}}{10}}-1}}{2\pi f_{ref}} = R_3C_3 \quad (5)$$

and

$$\tau_2 = \frac{(2\pi f_c)^{-2}}{\tau_1+\tau_3} \quad (6)$$

From the time constant, τ_3, given in the previous equation, it seems that the components R_3 and C_3 can be any combination, since the product R_3C_3 is τ_3. However, this is not true, e.g., it

is not wise to let C_3 to be higher that the other capacitances of the filter, because τ_3 ceases to be only dependent of R_3 and C_3 and becomes to interact with the other time constants. Thus, C_3 and R_3 must obey to:

$$C_3 \leq \frac{C_1}{10} \quad \text{and to} \quad R_3 = \frac{\tau_3}{C_3} \qquad (5)$$

The passive components were chosen using a custom template spreadsheet. Table I shows some specifications, LF components as well as the significant results, and it can be seen that the PLL has an almost fixed time to lock and independent from the division ratio, e.g., respectively about 10 µs and 7 µs for the first and second filters.

TABLE I: SPECIFICATIONS, LF COMPONENTS AND MOST SIGNIFICANT RESULTS.

	Filter 1			**Filter 2**		
Phase margin - ϕ_p [º]	45			55		
Bandwidth f_p [kHz]	900			900		
Frequency f_c [kHz]	589			540		
Attenuation *attn* [dB]	10			10		
C_1 [pF]	25			21		
C_2 [pF]	200			330		
R_2 [$k\Omega$]	3			3		
C_3 [pF]	2.5			0.7		
R_3 [$k\Omega$]	14			17		
N	**400**	**414**	**430**	**400**	**414**	**430**
Time to converge [µs]	10.6	10.8	11	7.3	7.6	7.7
Actual phase margin [º]	29.34	36.22	35.77	52.28	51.78	51.23
Actual freq. f_c [kHz]	594	286	279	271	264	256
Natural freq. f_n [kHz]	241	237	233	194	191	187
Dumping - ξ	1.823	0.448	0.444	0.605	0.594	0.583

III. RESULTS

Simulations and measurements made in the linear range, shown for the VCO a constant $K_{VCO} \approx 2.8$ [GHz/V], as well as the voltage-to-frequency (VF) characteristic of the Figure 5.

Simulations also shown for the charge-pump, *Up* and *Down* currents of I_{Up}=269 µA and I_{down}=201 µA, respectively, and a detector gain constant K_ϕ=75 µA/2π rad.

IV. CONCLUSIONS

This paper presented a frequency synthesizer for operation in the 5.7 GHz ISM band, whose chip layout is depicted in Figure 6, where are visible two PLLs. The synthesizer is a Phase-Locked Loop with a fixed division ratio, *N*, in the feedback path, whose value is digitally programmable from 0 to 15, in order to vary the division ratio from 400 to 430 in steps of 2 to produce the frequency range [5424; 5830 MHz] at the output, from the reference frequency of 13.56 MHz.

TSPC logic was used in order to make the power consumption lower as possible. The PLL was designed in the UMC RF 0.18 µm CMOS process and has an expected power consumption of 4.2 mW, from a power supply of 1.8 V.

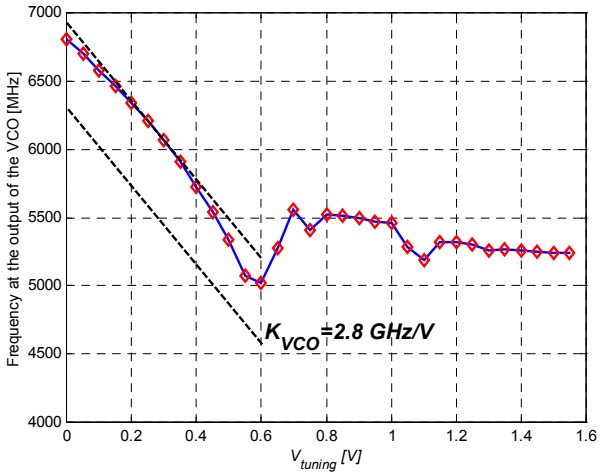


Figure 5: VF characteristic of the VCO.

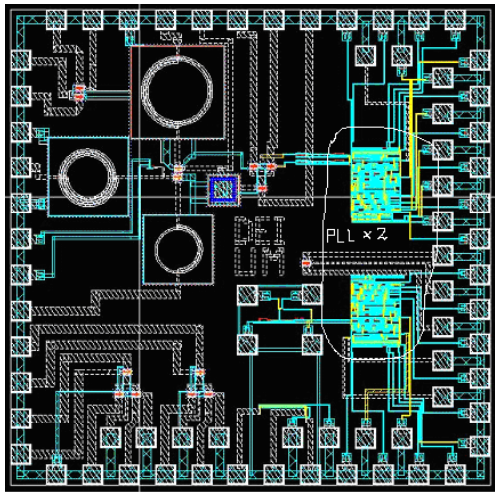


Figure 6: Chip layout, containing the RF transceiver for the transmission at 5.7 GHz and another PLL for testing purposes.

REFERENCES

[1] A. Abidi, "Phase noise and jitter in CMOS ring oscillators", IEEE Journal of Solid-Sate Circuits, Vol. 41, No. 8, pp. 1803-1816, August 2006.

[2] F. Gardner, "Charge Pump PLL", Transactions on Communications, Vol. 28, pp. 1849-1859, November 1980.

[3] C. Park, *et al*, "A low-noise, 900-MHz VCO in 0.6-um CMOS", IEEE Journal of Solid-State Circuits, Vol. 34, No. 5 pp.586-591, May 1999.

[4] B. Razavi, RF microelectronics, Prentice Hall, 1998.

[5] S. Pellerano, *et al*, A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic-frequency divider, IEEE Journal of Solid-State Circuits, Vol. 39, No. 2, pp. 378-383, February 2004.

[6] A. Hajimiri, T. Lee, "Phase Noise in Oscillators, A Tutorial", Invited Paper, IEEE Journal of Solid-State Circuits, Vol. 34, No. 3, pp. 326-336, March 2000.

[7] D. Banerjee, PLL performance simulation and design, 4th Edition, Dog Ear Publishing, 2006.

ACKNOWLEDGEMENTS

This work was supported by Foundation for Science and Technology FCT/PTDC/EEA-TEL/65286/2006 project.