High-resistivity polycrystalline silicon as RF substrate in wafer-level packaging

A. Polyakov, S. Sinaga, P.M. Mendes, M. Bartek, J.H. Correia and J.N. Burghartz

High-resistivity polycrystalline silicon (HRPS) is presented as a novel low-cost and low-loss substrate for radio-frequency (RF) passive components in wafer-level packaging and integrated passive networks. A record quality factor ($Q = 11$; 1 GHz; 34 nH) and very low loss (0.65 dB/cm; 17 GHz) are demonstrated for inductors and coplanar waveguides, respectively, on HRPS.

Introduction: Passive components, such as spiral inductors, transmission lines, and antennas, are limiting the performance and reduction of cost of integrated silicon radio-frequency (RF) systems. A major reason behind these limitations are the considerable substrate losses due to the conductivity of the silicon. This effect can only be reduced by increasing the silicon resistivity or by spacing the component away from the lossy silicon substrate [1]. Also, such components occupy a large fraction of the costly chip area.

A solution to these problems can come from an integration of the passive components over or under the active circuitry [2]. This can be accomplished by using a spacer substrate, having low RF loss, a high permittivity, and good thermal conductivity. This spacer substrate is inserted in between the active chip and the passive components and can be applied in wafer-level packaging (WLP), as shown in Fig. 1.

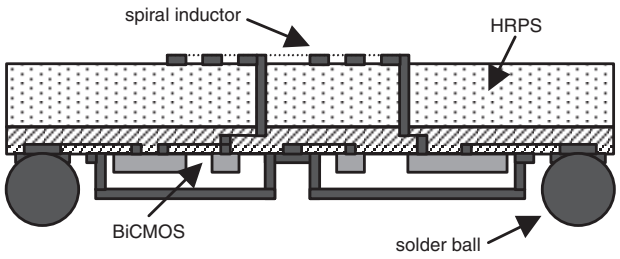

Fig. 1 *Conceptual wafer-level chip-size package based on low-loss high-resistivity polysilicon (HRPS) serving as mechanical carrier and vertical spacer for passive component integration over integrated circuit wafer*

Glass substrates that have been proposed for passive component integration could be considered for this purpose [3]. Glass, even though used in WLP for some applications [4], has, however, a low dielectric constant and a poor thermal conductivity. Silicon is superior in both aspects and can provide low loss figures if high-resistivity silicon (HRS; 1–10 kΩ cm) is used [5]. Single-crystalline float-zone HRS wafers, however, are expensive and prone to surface-channel effects unless an additional surface-passivation step is added [5].

In this Letter, high-resistivity polycrystalline silicon (HRPS), which can be adopted from the early phase of float-zone wafer preparation (wafers from high-resistivity polysilicon rods), is proposed as a novel cost-effective alternative to glass and HRS RF substrates.

Test structures: Coplanar waveguides (CPWs), which are particularly sensitive to surface effects, were used as test structures to evaluate the RF losses of glass, HRS and HRPS substrates. A CPW T-resonator and a large (34 nH) spiral inductor were included with that test site as well. A 2 μm-thick aluminium (Al) metallisation was used in all cases. CPWs on the HRPS were formed with and without a 1 μm-thick PECVD oxide isolation layer. The HRS wafers had an oxide isolation with or without a surface passivation [5]. Three types of glass substrates were included with our evaluation, i.e. Pyrex 7740, Hoya SD-2 and Schott AF45. The CPW test structures were designed with different signal-ground spacings in order to achieve impedances close to 50 Ω in all cases and to allow for meaningful comparisons. CPW length of 0.5, 1, 3 and 5 mm were used.

Results and discussion: The dielectric constant (Fig. 2*a*) and the total loss (Fig. 2*b*) were obtained from *S*-parameter measurements up to 10 GHz. Good agreements of the measured data and simulations in ADS-Momentum were obtained for all CPW structures and substrates shown in Fig. 2. In comparison to the glass substrates, i.e. Pyrex 7740 ($\alpha = 0.7$ dB/cm), Hoya SD-2 ($\alpha = 0.37$ dB/cm) and Schott AF45 ($\alpha = 0.38$ dB/cm), a comparably low loss figure was measured for HRPS with ($\alpha = 0.44$ dB/cm) and without ($\alpha = 0.89$ dB/cm) an insulation oxide layer at 6 GHz. Given this result, HRPS offers several advantages in comparison to glass, such as the higher and nearly frequency independent dielectric constant (11.7 against 4.8–6.2; Fig. 2*a*) allowing for a 30–35% more compact component integration, the >10-times higher thermal conductivity, the perfect matching of the thermal expansion coefficient to that of the integrated circuit (IC) wafer, and the full compatibility with silicon processing. The fact that a low loss tangent could be demonstrated for HRPS without an insulation oxide layer is significant, because metal vias through the HRPS substrate can therefore be built without any complicated dielectric liner formation (Fig. 1). In comparison to HRS, no additional surface passivation steps are required for HRPS, as seen from the 30 GHz *S*-parameter data in Fig. 3; that is, because the material has an inherently high defect density (Fig. 4), suppressing any surface channel formation similarly to the surface amorphisation to passivate the HRS [5]. Moreover, CPW T-resonators having quality factors $Q = f_0/f_{3\text{-dB}} > 18$ demonstrated the low loss of HRPS, while eliminating any de-embedding error. High *Q*s of 7.5 and 11 were measured for the 34 nH spiral inductor with and without an insulating oxide layer, respectively, thus providing further evidence of the excellent RF quality of the HRPS substrate.

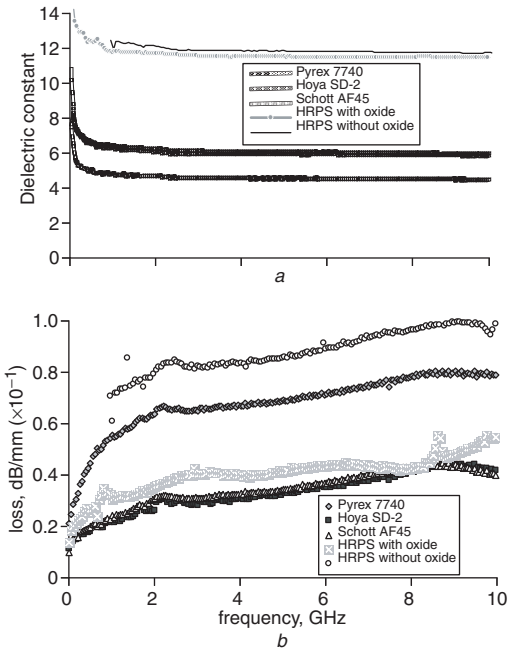

Fig. 2 *Measured frequency dependence of dielectric constant and loss tangent for three types of glass substrates and for high-resistivity polysilicon (HRPS) with and without insulating oxide layer*

a Dielectric constant
b Loss

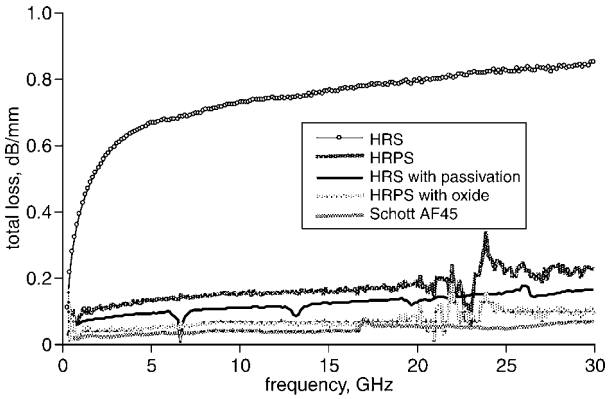

Fig. 3 *Frequency dependence of total loss of coplanar waveguides on high-resistivity polysilicon (HRPS) in comparison to high-resistivity single-crystalline silicon (HRS) with and without surface passivation and to Schott AF45 glass substrate*

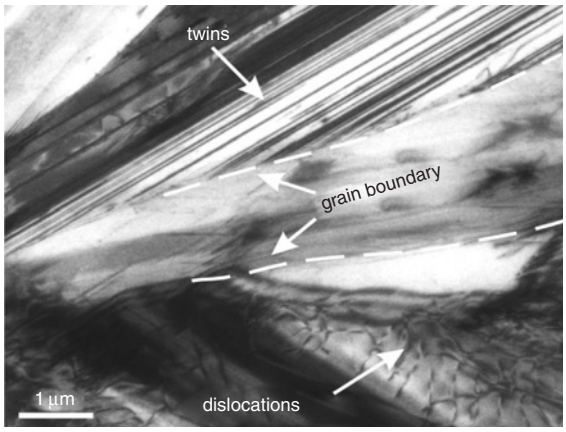

Fig. 4 *Plan-view transmission electron micrograph*

Conclusion: HRPS has been presented and demonstrated as a novel RF substrate for wafer-level packaging and passive component integration in general. The material provides very low RF loss compared to that of glass, a high dielectric constant to allow for compact passive component integration, a high thermal conductivity, and a perfect match of the thermal expansion coefficient to that of the IC wafer. Finally, HRPS is fully compatible with silicon processing and is a low-cost alternative to HRS wafers.

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