Smart Load Cells Based on Switched-Capacitors

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ABSTRACT

This paper describes a data acquisition solution using a single chip RISC type microcontroller with very few other active and passive components around, taking advantage of the ratiometric functioning of the load cells. The need for thermally stable circuits and components is minimized through the use of the same amplification chain for both signal and reference, together with software calibration. The amplification and filtering is done through switched-capacitors techniques, controlled by the microcontroller. This option allows the choice of the proper scale according to the platform, with periodical and automatical calibration. The analog-to-digital conversion is done using the single ramp approach controlled by the microcontroller, which does all the digital processing required as well as the serial communication with the external world. The paper also describes an example of software calibration of a multi-loadcell weighbridge, using one single processing module per sensor.

Key Words: Instrumentation, Smart Sensors.

INTRODUCTION

Multi-load-cell weighing systems using 4 or 6 load cells under a platform (mechanical paralleling), normally use a single signal processing circuit with the individual load cells outputs tied together (electrical paralleling). Because this electrical paralleling, the tuning of the gain of a load cell affects the behavior of the others, calibration is difficult and tedious, specially with weighbridges for car and trucks, requiring the motion of heavy weights around large platforms.

The use of load cells with digital outputs, i.e., with integrated signal processing, allows the gain adjustment to be a simple multiplication of the load cell output by a coefficient, operation which does not affect the other load cells outputs. In this case, the calibration process means the calculation of the multiplying coefficients, which are given by the solution of a set of equations, operation easily performed by any general purpose microcomputer.

However, this solution needs a cost effective signal processing circuit including amplification, A-to-D conversion and networking capabilities.

Having in mind industrial weighing applications where 6000 divisions are needed for the equipment (external divisions) a conversion resolution of at least 60000 divisions (10 internal divisions for each external) with 50 or more readings per second, at least for static weighing applications. For dynamic weighing a faster reading rate is required but with lower resolution.

For the specifications referred there are already suitable components in the market, namely amplifiers and A-D converters [1,2], some of these even with networking facilities [2]. However some other facilities toward intelligent sensing [3,4] are also desirable: amplifier gain and offset adjustment controlled by software, scaling and eventually digital filtering of the converter results. These requirements need processing capabilities. Once the microprocessor is needed, the all architecture should be rethought in order to maximize its use, reducing the hardware and its specifications.

This contribution describes a feasibility study towards a solution for the problem taking advantage of the high performance low cost microcontrollers available today and of the ratiometric functioning of the load cells [2].

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SIGNAL PROCESSING CIRCUIT

Design Strategy

Fig. 1 shows the conceptual ideas behind the proposed circuit.

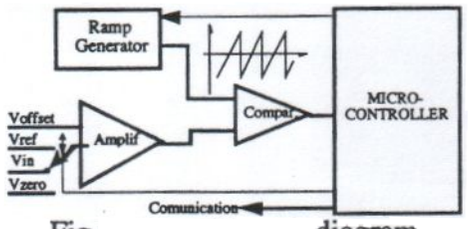

Fig. diagram

The same amplifier chain is properly switched to deal with the zero, the load cell signal and the conversion reference. In this way the thermal stability requirements for the amplifier can be relaxed as a change in gain will affect all the three entities defining the A-D conversion. A simpler architecture can be used just enough to ensure that the gain remains constant during the conversion period.

A single ramp conversion was used because it requires the minimum hardware and it allows a higher rate of conversions. However this simple conversion technique is not intrinsically compensated as dual ramp conversion for example, requiring some pos-conversion processing specially in this case where the zero, the signal and the reference are allowed to change.

The counting associated with the single ramp A-D conversion, the control of the switches in the amplifier stage and the control of the ramping capacitor discharge are tasks to be performed by a microprocessor architecture. Some number crunching to work out the conversion result, which may include scaling, eventually some digital filtering and the communication with the outside world, are the other tasks to the microprocessor

Fig.2 shows the conversion process and the related calculations required. To minimize the hardware and to reduce the errors the same comparator is used to detect the three level crossings. Normally these comparisons are done one on each ramp, therefore requiring three ramps [1]. In this case the three comparisons are done during the same ramp reducing the conversion time to a third. All it is needed, is to allow enough time to switch the amplifier chain from one signal to the other, until there is stable output. This was accomplished in the conversion by restricting (Vinmin-Vzero) and (Vref-Vinmax) to be $\geq \Delta V$ volts to allows the transients to settle. With this strategy the Vin range is reduced but the precision of the conversion is improved as the denominator is increased, as can be seen in the expression giving the conversion result.

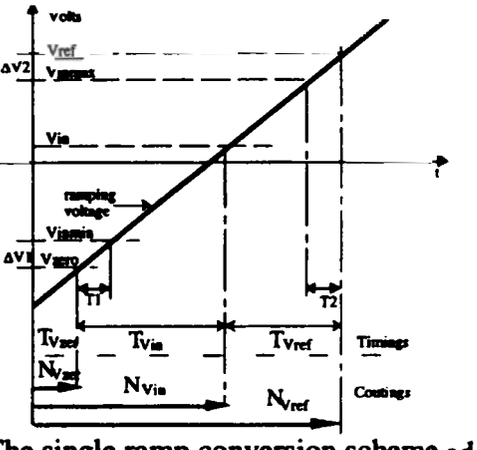

Fig.2- The single ramp conversion scheme adopted

The conversion result is given by the expression below, where N_{Vzero}, N_{Vin}, N_{Vref} represent the time for ramp to reach the zero, signal voltage and reference. N_k is a normalizing factor.

$$\text{Conversion} = \frac{N_{Vin} - N_{Vzero}}{N_{Vref} - N_{Vzero}} \times N_k$$

Circuit Implementation

Fig.3 shows the circuit implemented for this feasibility study comprising the digital processor/controller, the amplifier and the conversion.

The Controller: The circuit was developed around an 8 bit single chip Harvard architecture microcontroller with RISC-like features, the PIC17C42, with interesting characteristics for this type of applications:

- operating speed: DC - 20 MHz clock input (200ns instruction cycle).
- Low cost.
- Small size with EPROM.
- Low power consumption.
- Three 16-bit timer/counters.

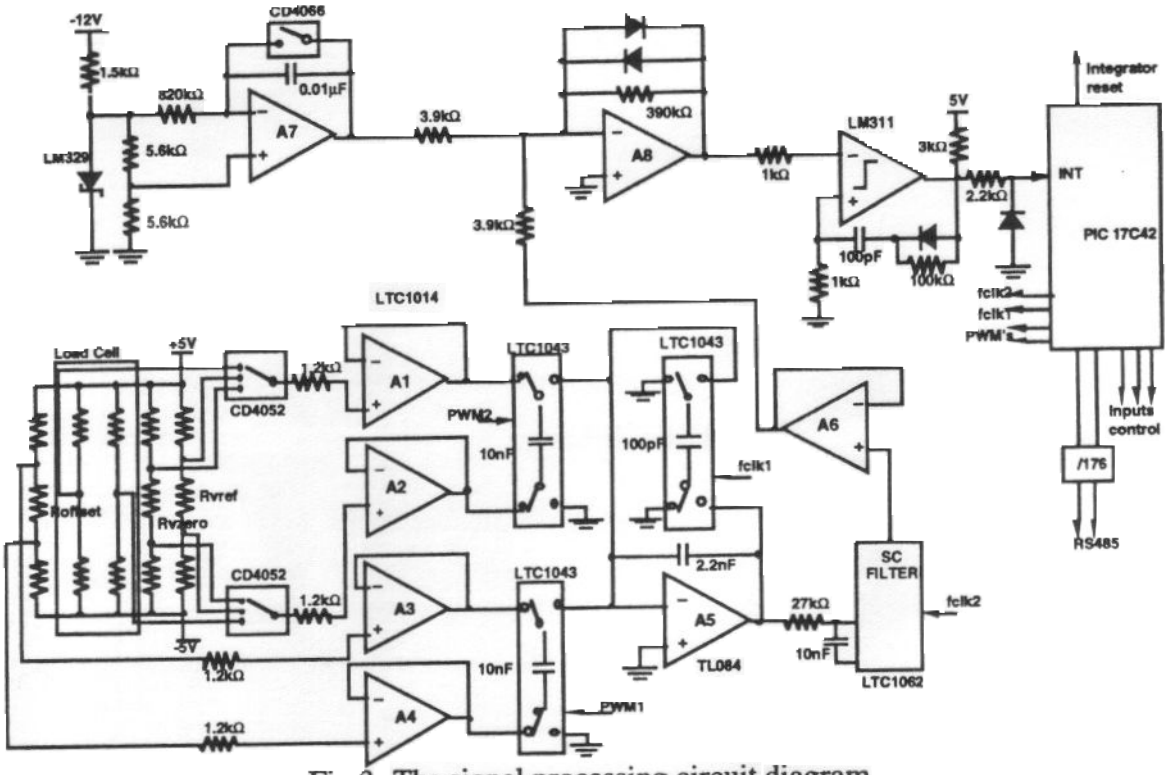

Fig.3- The signal processing circuit diagram

The Amplifier Stage: An instrumentation amplifier (gain programmable by software) was built with Switched-Capacitors techniques. Three SC blocks, controlled through PWM's outputs of the microcontroller, amplify the input signals (Vzero, Vin, Vref) and the offset. On charge manipulation was used capacitors of polystyrene [5] (low drift). The gain stability was guaranteed by high precision of PWM's output frequency. Filtering after amplification was achieved with a SC filter (low-pass, 5ºorder) with cut-off frequency programmable through a digital signal from the microcontroller. The amplification result is given by the next expression:

$$Vo5 = \frac{10nF * f_{PWM2}}{100pF * f_{clk1}} * Vsinal - \frac{10nF * f_{PWM1}}{100pF * f_{clk1}} * Voffset$$

The inputs of the instrumentation amplifier is switched between zero, the load cell and the reference voltage through a dual 4-to-1 multiplexer (CD4052) driven by the microcontroller. The zero signal and the reference are given by a voltage divider across the load cell feeding voltage. The voltage divider resistors were chosen with very low temperature coefficient, while the others are the common metal film resistors with ±50ppm/ºC.

The Ramp Generator: The integrator circuit built with A7 implements this function. The switch CD4066 driven by the PIC17C42 discharges the capacitor to restart the ramp. To have a stable slope the reference zener voltage LM329 was used to define the integrating current. Also a polypropylene integrator capacitor, with low dielectric absorption, was used to guarantee the constant slope independent of the A7 output voltage.

The Comparator: To assure a faster and more sensitive comparison the opamp A8 was used, so that at the A8 input summing point, the current due to the ramp is subtracted from the current proportional to the signal. When this current difference is large A8 operates at a low gain due to the diodes in the feedback loop. When the currents produced by the ramp potential and A6 very nearly balance, the potential at A8's summing junction will go low enough, so that A8 comes out of the diode bounding and operates with a gain determined by the feedback resistor (390kΩ) [1]. The A8 makes the comparator's job much easier, as it amplifies by a factor of 100, the voltage difference between the

two signals, reducing the A8 input uncertainties. The components in the positive feedback path at A8 ensure a sharp transition.

CALIBRATION PER SMART LOAD CELL

A scale with a steady zero and reference, limits the maximum excursion of the load cell output, to accommodate platform changes. A promising solution for all kind of platforms was tested with automatical and periodical calibration. After estimate platform's weight and obtain the gain for the input signals, the system is ready for weighings. The 1st conversion is useful to evaluate the gain for input signals and the offset. An example about this is shown:

1st CONVERSION:

Vzero=10mV; Vref=30mV; Voffset=-20mV.

Scale: -2Vto 2V.

On a 1st conversion, a gain of 200 was used for the inputs signals and the offset (to settle the scale). The measurement of the platform's weight is used to define the gain for the following conversions (see Fig.4).

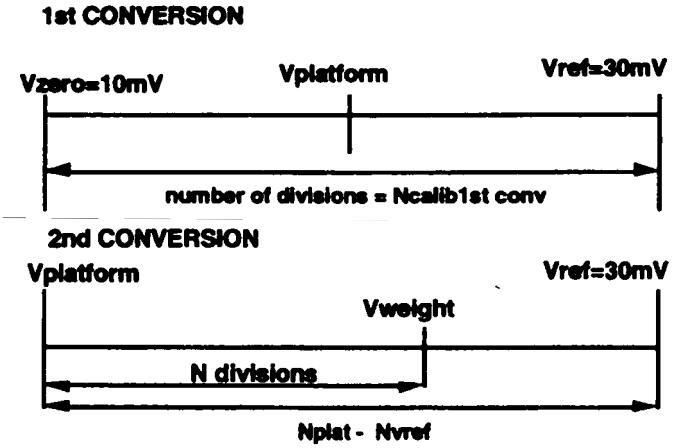

Fig. 4 - Example for one weighing

$$\text{Conversion} = \frac{N}{Nplat - Nvref} \times N_k$$

On a 2nd conversion only two signals (Vweight e Vref) were amplified for obtain Nweight e Nvref. The 1st calibrating conversion, followed by weighing conversions, needs to be repeated periodically, every 10 readings. The calibration consists on the determination of number of countings - Ncalib (Nzero-Nvref) - and on the adjustment of the gain to set for following conversions.

EXPERIMENTAL RESULTS

The microcontroller driven by a clock frequency of 16MHz (250ns instruction cycle) gives a counting period of 250ns. The integration components, R=820kΩ and C=10nF gives the described by the equation:

$$V_{o7}(t) = -3.445 + 420.12t \quad (t \text{ in sec})$$

Filtering problem due SC gain control was solved with two filtering time constants for the SC filter:

- a short time constant to enable rapid transitions of A6 output;
- a large time constant to minimize the A6 ripple;

Fig.5 shows A6 output during a transition from Vin to Vref (cut-off frequency higher).

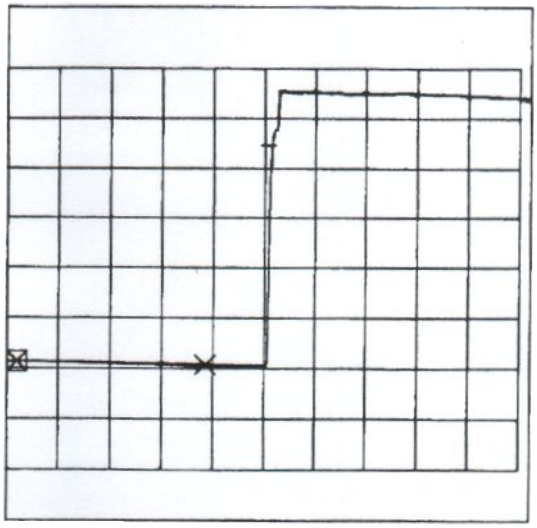

Fig.5 - Screen plot of A6 output.
Ch1 0.5mV/div = A6 output.
Time base 0.5ms/div.

In Fig.6 a screen plot of a Tektronix 2230 digital oscilloscope presents the A7 ramp output and the A8 output, before and after the crossing occurs, with the three pulses.

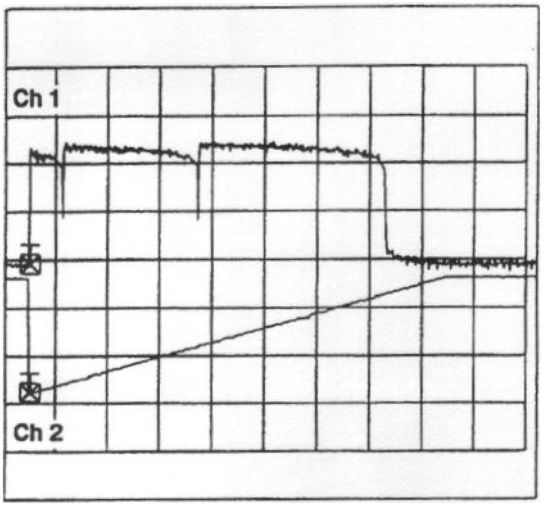

Fig.6 - Screen plot of A7 and A8 outputs.
Ch1 1V/div = A8 output.
Ch2 2V/div = A7 output.
Time base 2ms/div.

Fig.7 shows an example for a given Vin and Vref, waveform Ch2 is the instrumentation amplifier output, illustrating the input signal switchings, and the Ch1 waveform is the ramp.

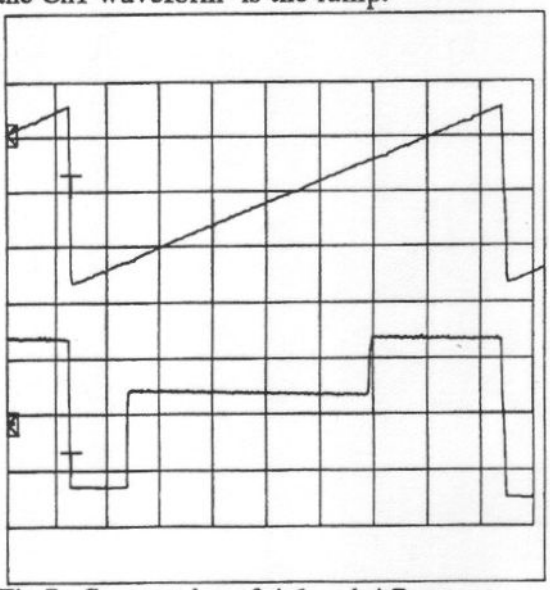

Fig.7 - Screen plot of A6 and A7 outputs.
Ch1 2V/div = A7 output.
Ch2 2V/div = A6 output(INV).
Time base 2ms/div.

The next table shows the sets of conversion results for different inputs.

INPUTS mV	12,02	21,25	23,75	27,87
RESULT CONV	31652	56079	62623	73538
	31657	56078	62625	73531
	31650	56081	62620	73525
	31642	56071	62614	73523
	31640	56086	62621	73522
	31641	56087	62617	73539
	31645	56084	62612	73524
	31653	56079	62609	73529
	31656	56078	62614	73528
	31648	56081	62608	73539
Average	31648	56080	62616	73531
Deviation	-8, +9	-9, +7	-8,+9	-9,+8

The conversion time obtained was around 18ms, time which can be reduced by increasing the microcontroller clock frequency up to 25 MHz. The resolution attained of 60000 divisions can also be increased.

SOFTWARE CALIBRATION

To test the software calibration method for the multi-load cell weighbridges, it was decided to use standard readout units instead of the prototypes above referred. A local weighing equipment manufacturer made available two 4 load cells platforms and 8 digital readout units with networking facilities. Load cells taking a maximum nominal weight of 100kg, with 3000div resolution and a sensitivity around 2mV/V, were used. The 4-load cell platforms coupled to a single readout unit is rated to 200kg with a resolution of 100gr. Each of the readout units were calibrated to give around 60kg with a 20gr resolution.

Two sets of tests were done, one for a 4 load cells platform, and another for a 8 load cells system, using two 4 load cells platforms.

The calibration method consists on doing N readings of weight on each load cell obtained by moving a mass with a known weight around the platform. The number of readings is the same as the number of load cells under the platform. The best results are given by the N readings obtained, concentrating the weight as much as possible above each one of the N load cells.

For the 4 load cells platform 4 sets of 4 readings were made, and the weights found were used to

workout the multiplying coefficients. These factors affecting each one of the readings, enables the correct evaluation of the weight above the platform. A system of 4 equations and 4 unknowns was built:

$$K_1W_{11} + K_2W_{12} + K_3W_{13} + K_4W_{14} = W$$
$$K_1W_{21} + K_2W_{22} + K_3W_{23} + K_4W_{24} = W$$
$$K_1W_{31} + K_2W_{32} + K_3W_{33} + K_4W_{34} = W$$
$$K_1W_{41} + K_2W_{42} + K_3W_{43} + K_4W_{44} = W$$

The solution of this system gives the K factors required to evaluate the weight of an unknown mass.

With the following W_{rc} readings calculated with a calibrated mass of 20kg positioned in four different places:
- W_{1c} readings 3.86, 9.96, 6.82, 0.72;
- W_{2c} readings 1.74, 2.94, 10.88, 5.58;
- W_{3c} readings 4.50, 0.74, 3.54, 13.26;
- W_{4c} readings 13.30, 2.92, 1.48, 4.38;

the K_c factors evaluated:

$K_1 = 0.90025$, $K_2 = 0.91580$, $K_3 = 0.99196$, $K_4 = 0.88685$.

Using these factors several (25) weighing operations were done, with different masses (1, 5, 20 up to 80kg), located in different points of the platform, having been recorded very encouraging results, with errors below 50gr (4000 divisions in 200kg).

For the composite platform with 8 load cells the test was repeated and the 8 multiplying coefficients were calculated. The weighing tests done confirmed the approach followed giving errors below 100gr, i.e. again 4000 divisions in 400kg.

CONCLUSIONS

The architecture tried had shown to be able to give the required performance at a very reasonable cost. The implementation of smart load cells including self-calibration and networking facilities seems achievable and cost effective even for multi-load cells applications, where considerable reduction on the commissioning time, through the software system calibration, is highly interesting. Once the circuit is fully tested it is planned to produce an ASIC including most of the circuit components.

ACKNOWLEDGMENTS

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REFERENCES

[1] "A 20 - bit (1ppm) Linear Slope Integrating A/D Converter", Application Note 260, National Semiconductor.

[2] "Intelligent Signal Processing for Ratiometric Data Acquisition: A Low Cost Solution for Load cells", C. Couto, J. Higino, Proceedings of IMEKO TC-4, Brussels, Belgium, 1993.

[3] "Integrated Smart Sensors", J.H. Huijsing, Sensors and Actuators, Vol A30, pp167-174, 1992.

[4] "Modelling of Smart Sensors: Application to a Smart Temperature Transmitter", J. M. Riviére, M. Robert, C. Aubrun, Proceedings of IMEKO TC-4, Brussels, Belgium, 1993.

[5] "A Switched-Capacitor Interface for Capacitive Pressure Sensors", M. Yamada, K. Watanabe, IEEE Trans. Instrum. Meas., Vol. IM-41, pp.81-86, 1992.