

A 5.7 GHz RF transceiver for wireless sensors applications

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Abstract — This paper presents a radio-frequency (RF) transceiver fabricated in a UMC RF 0.18 μm CMOS process. The RF transceiver was built to operate at the 5.7 GHz ISM band. The transceiver has a total power consumption of 23 mW and it is intended for the use in each wireless node of a wireless sensor network.

I. INTRODUCTION

Wireless communication microsystems with high density of nodes and simple protocol are emerging for low-data-rate distributed sensor network applications such as those in home automation and industrial control [1]. It is available a huge range of solutions, concerning the implementation of wireless sensors networks. A few companies [2-4] are offering products such as motes and sensor interfaces. The motes are battery-powered devices that run specific software. In addition to running the software networking stack, each mote can be easily customized and programmed, since it runs open-source operating systems which provides low-level event and task management. Mote Processor/Radio module families working at 2.4 GHz ISM band and supporting IEEE802.15.4 and ZigBee are available [2-4]. However, the implementation of a wireless bus in certain applications requires compact and miniaturized solutions. Moreover, a chip-size antenna included in the RF microsystem will be crucial. In order to implement efficient power-consumption wireless sensor networks, it is necessary to develop a low-power/low-voltage RF transceiver, suitable to be mounted with a patch antenna. In wireless communications, the antenna is one of the most critical subsystem, thus, in order to not compromise the desired miniaturization, the antenna must be small enough to comply with size constraints of the microsystems. The investigation of new frequency bands [5] and new geometries [6] will make possible to have smaller antennas to integrate in wireless microsystems [7,8]. This makes the chose of the most suitable frequency, one of the more decisive aspects in the design of RF transceivers. Normally, the desired range, baud-rate and power consumptions are key-aspects in the design to take in account, when the frequency of operation is to be selected. At a start-up point, the range limits the maximum usable frequency, because the loss suffered by the radiowaves in the free-space increases with the distance. However, to keep or even increase the useful life of the batteries, such a variation in the transmitted power is not possible to do. Moreover, in the case of applications requiring higher baud-rates, the transmitted bandwidth must also be higher, in order to support these applications.

However, the frequency can't be arbitrarily increased, because this have implications in the power consumptions, e.g., at high frequencies, the transistors must switch faster, thus the energy dissipation will be bigger.

Figure 1 shows the available frequency bands for the different technologies used in wireless communications. The most suitable frequencies are those belonged to the so called ISM band (Industrial, Scientific and Medical), due to its unregulated usage, e.g., these frequencies are not subjected to standardization and can be freely used, since the emitted power are maintained below the maximum levels imposed by the legislation. Such a flexibility leaded to the rising and spreading of interesting applications. The target application of microsystems using the proposed 5.7 GHz RF transceiver in this paper, is the implementation of a wireless sensors networks.

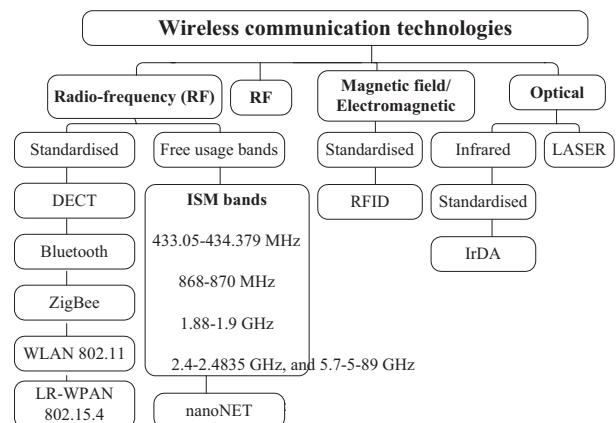


Fig. 1: Frequency bands and respective applications.

II. RF TRANSCEIVER DESIGN

A. Architecture

It was fabricated a RF CMOS transceiver operating at 5.7 GHz ISM band, with ASK modulation. The UMC RF 0.18 μm CMOS process allows to trade the high-frequency capability of minimum-length transistors with lower current consumption by biasing the devices at lower current densities, even for devices working at RF. This process provides a poly and six metal layers, the use of integrated spiral inductors (with a quality factor of ten), high-resistor values (a special layer is available). The transceiver has a low-noise amplifier (LNA) that provides a 50 Ω input impedance, the amplified RF signal is directly converted to the baseband with a single balanced active MOS mixer. The internal oscillator is a Phase-Locked Loop (PLL) working at 5.7 GHz. The transceiver's structure is illustrated in Figure 2.

is $N=2(M.P+S)$, where $(M+1)/M$ (with $M=10$) are the variable frequency divider ratios of the prescaler, $S=20$ is the divider ratio of the main counter, and S is the divider ratio of the swallow counter. The main counter has a divider by $P/2=10$ followed by a toggle flip-flop, which makes the feedback signal at the divided input, f_{div} , of the PFD to have a duty-cycle of 50% (as it happens with the reference signal at the main input, f_{ref} , of the PFD). Compared with other situations, where the PFD's inputs have different duty-cycles, this minimises possible delays that can arise, during the locking process of the PLL. This is of special concern in situations when the PLL is turned on or after an order to switch the frequency at its output.

Figure 6 shows the structure of the TSPC frequency divider by two and prescaler. The frequency at the input of the prescaler is in the range [2712; 2915 MHz], and previous measurements shown for this technology that for frequencies above 2 GHz, it exists an impossibility to make frequency division with the use of static logic. Thus, TSPC logic must be used in order to make work the further circuits in static logic. The TSPC logic was used again to overcome the impossibility to implement the first stage of the prescaler (the frequency divider by 2/3 with modulus control) with static logic in this technology. However, in order to the TSPC

dividers work properly, the inputs must be rail-to-rail.

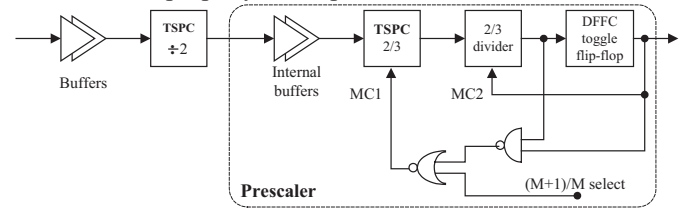


Fig. 6: The block diagram of the buffers, the TSPC divider by two, followed by the prescaler.

In the global structure of the frequency divider, the swallow counter plays an important role, e.g., the fixed division by 10 or 11 is extremely easy to achieve. The difficulty is to establish the precise intervals in which the division must be made and why. Figure 7 shows three situations of divisions give by $200=(15 \times 10)+5 \times 10$, $203=(3 \times 11+12 \times 10)+5 \times 10$ and $215=(15 \times 11)+5 \times 10$ (for the global divisions of 400, 406 and 430), as well as the behaviour of the $(M+1)/M$ control signal to the prescaler. The CLK signal is the signal at the output of the VCO, VCOout, after to be divided by two in the TSPC frequency divider, thus, this is why half of the countings are referred and not the exact value.

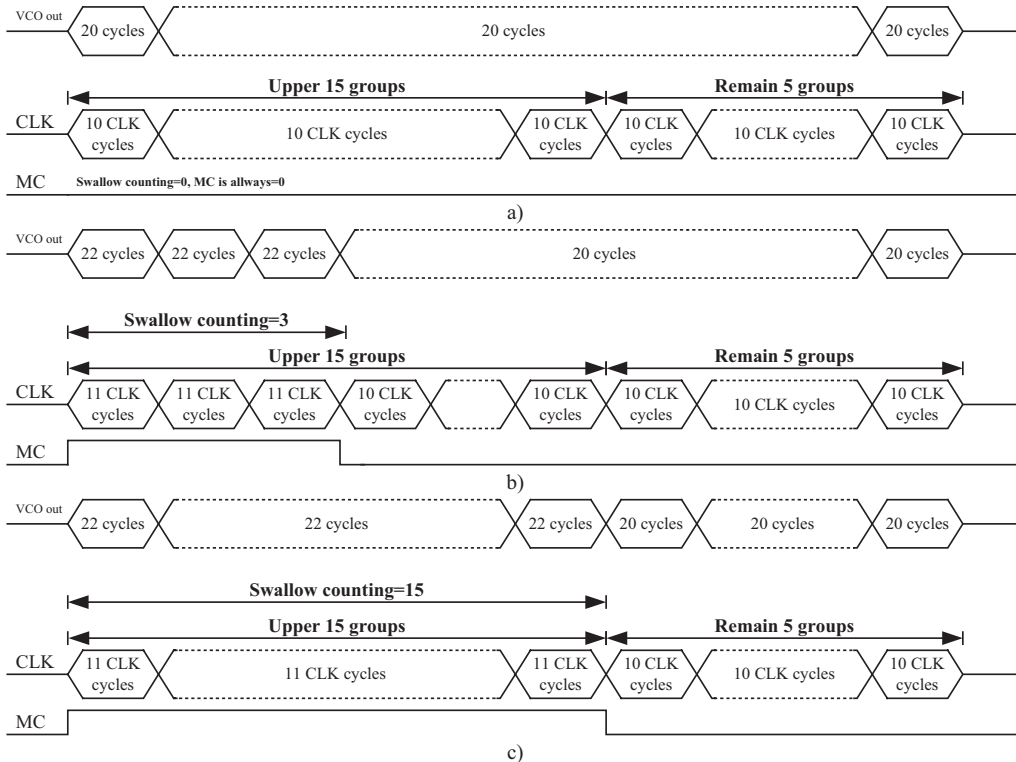


Fig. 7: Swallow counting process to generate the appropriate MC signal for the prescaler, for three global division ratios: a) 400, b) 406 and c) 430

Basically, the idea behind the frequency division is the definition of a general rule to simultaneously make the division of the minimum to the maximum in steps of one (in this case, from 200 to 215), and further in steps of two. In this case, the difference between the two limits is 30 and the

swallow counting is from 0 to 15, so the values $11 \times S + 10 \times [\max(S) - S] + 50$, with $S \in \{0, 1, \dots, 15\}$ and $\max(S) = 15$ will be a useful solution to the problem. Then the final division ratios in steps of two, are ensured by the first TSPC toggle flip-flop, at the same time the last static toggle

flip-flop in the main counter, P , ensures that the divided signal has a duty-cycle of 50%. The swallow counter is essentially a descendent programmable counter and it operates as follows: the counter is initiated to the desired value S , and then it starts to counting in the descending order until zero. Meanwhile, the MC signal is activated, then it falls down, except when S is already initialized at zero.

III. EXPERIMENTAL RESULTS

At frequencies in the range [5.420-5.830 GHz], the experimental results of simulations shown for the LNA a gain in the range [9.597-9.807 dB], a stabilization factor K of 1.209, making the LNA unconditionally stable ($K > 1$). The VCO has a constant $K_{VCO} \approx 2.8$ [GHz/V], obtained from the linear range, as well as the voltage-to-frequency (V/F) characteristic of the Figure 8. The charge-pump has Up and $Down$ currents of 269 μ A and 201 μ A, respectively, and a detector gain constant $K_{\phi} = 75$ μ A/ 2π rad. The up and $down$ currents of 269 μ A and 201 μ A, respectively, and a detector gain constant $K_{\phi} = 75$ μ A/ 2π rad. The LNA shown a power consumption of 9.65 mW.

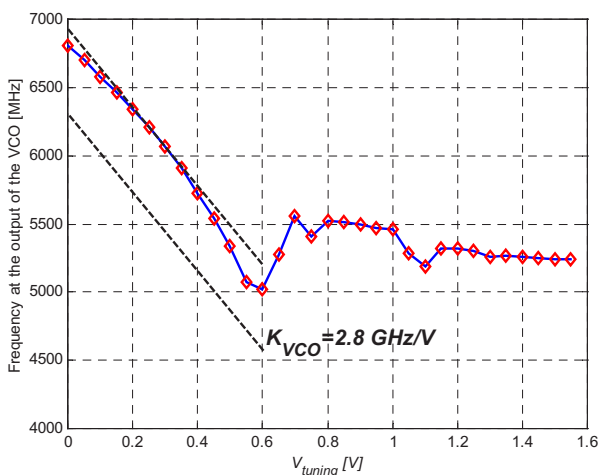


Fig. 8: V/F characteristic of the VCO.

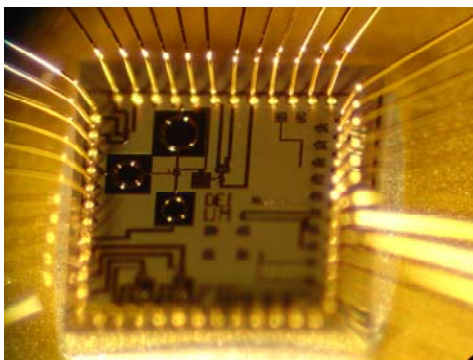


Fig. 9: A photo of the RF transceiver for the 5.7 GHz.

The simulations also shown power consumptions about of 9.51 mW for the mixers, and 4.14 mW for the PLL. A photo of the fabricated transceiver used for the transmission at 5.7 GHz is depicted in Figure 9.

IV. CONCLUSIONS

A low-power RF transceiver for a wireless EEG single-electrode module was fabricated in a UMC RF CMOS 0.18 μ m process. The RF transceiver was built to operate at the 5.7 GHz ISM band. Simulations shown for the RF transceiver, a total power consumption of 23 mW. The target application of the RF transceiver, is for use as low-power nodes, in wireless sensors networks.

This paper dealt essentially with the design of the receiver. The full characterization of the receiver, as well as the full experimental testing of the receiver and the PLL, are tasks of future work.

REFERENCES

- [1] P. Choi, *et al*, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4 GHz", IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, pp. 2258-2268, December 2003.
- [2] Crossbow Inc., www.xbow.com.
- [3] Dust Networks Inc., www.dust-inc.com.
- [4] Sencicast Systems, www.sencicast.com.
- [5] E. Callaway Jr., Wireless sensor networks, Architectures and protocols, Chapter 3: The physical layer, CRC Press, 2004.
- [6] E. Mackensen, *et al*, "Enhancing the lifetime of autonomous microsystems in wireless sensor actuator networks (WSANs)", in Proc. of the XIX EuroSensors, Barcelona, Spain, 2005.
- [7] J. Gutierrez, *et al*, "IEEE 802.15.4: Developing standards for low-power low-cost wireless personal area networks", IEEE Network, pp. 2-9, September 2001.
- [8] C. Enz, *et al*, "Ultra low-power radio design for wireless sensor networks", in Proc. IEEE International Workshop on Radio-Frequency Integration Technology: Integrated Circuits for Wideband Communication and Wireless Sensor Networks, Singapore, December 2005.
- [9] G. Montagna, *et al*, "A 35-mW 3.6-mm² fully integrated 0.18- μ m CMOS GPS radio", IEEE Journal of Solid-State Circuits, Vol. 39, No. 7, pp. 1163-1171, July 2004.
- [10] S. Pellerano, *et al*, "A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic-frequency divider", IEEE Journal of Solid-State Circuits, Vol. 39, No. 2, pp. 378-383, February 2004.