Low-power low-voltage RF CMOS transceiver at 2.4 GHz

J. P. Carmo[χ], P. M. Mendes[ξ], C. Couto[ξ], J. H. Correia[ξ]
[χ]Polytechnic Institute of Braganca, ESTiG, Campus Santa Apolonia, 5301-857, Braganca, Portugal
Phone: +351-273-303000, Fax: +351-273-313051, e-mail: **jcarmo@ipb.pt**
[ξ]University of Minho, Dept. Industrial Electronics, Campus Azurem, 4800-058, Guimaraes, Portugal

***Abstract* — A radio-frequency transceiver chip was designed in a UMC RF 0.18 μm CMOS process. The target RF frequency is 2.4 GHz ISM band. A possible application of this transceiver is the integration into textiles for sensing biomedical data. The power supply of the transceiver is 1.8 V. Simulations shown power consumption less than 10 mW for the receiver.**

I. INTRODUCTION

CMOS technology has reached its maturity. Therefore, design engineers used it for developing RF circuits. The advantages of CMOS technology are the higher integration, low-power consumption, low-voltage supply and low-cost compared with Bipolar technology. The use of CMOS process with low length for the channels of the MOSFETs is very important for high-frequency devices.

This paper describes a radio frequency transceiver designed in UMC RF 0.18 μm CMOS process. This process has a poly and six metal layers, allowing the use of integrated spiral indutors (with a reasonable quality factor), high resistor value (a special layer is available) and a low-power supply of 1.8 V.

The transceiver has a low noise amplifier that provides a 50 Ω input impedance, using a tuned load to provide high selectivity. The amplified RF signal is directly converted to the baseband with a double-balanced downconversion mixer, using a switched transconductor mixer. It's intended to drive the 50 Ω output load with an optional source follower device. Internal oscillator is a Phase-Locked Loop (PLL) working at 2.4 GHz, with a stable crystal oscillator reference of 20 MHz. The whole transceiver structure is illustrated in Fig. 1.

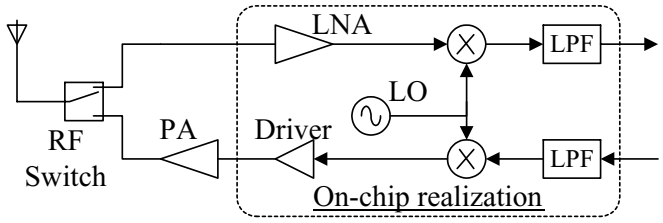

Fig. 1. The block schematic of the transceiver.

This RF CMOS transceiver will be applied in a wireless electronic shirt for helping health professionals with rapid, accurate and sophisticated diagnostic concerning cardiopulmonary disease in order to evaluate the presence of breathing disorders in free-living patients.

II. TRANSCEIVER

A. Low-noise amplifier

LNA is an indutively degenerated common source amplifier with tuned load and cascode transistor [1,2]. This makes the input impedance at 2.4 GHz equal to 50 Ω, for matching with antenna switch. Fig. 2 illustrates this circuit:

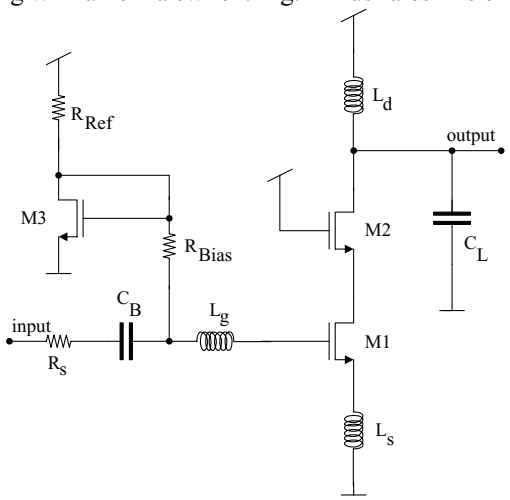

Fig. 2. LNA circuit [1,2].

B. Phase-locked loop

As depicted in Fig. 3, the PLL has a reference generator circuit with a crystal based oscillator at 20 MHz, followed by a Phase-Frequency Difference Circuit (PFD) without dead zone, a current steering charge pump (CP), a third order passive filter. The passive section output is connected to the VCO, that generates the desired frequency of 2.48 GHz. Finally, in order to get the 2.48 GHz, this frequency must be divided by 124 and connected to the PFD again, closing the loop.

C. Charge pump

The charge pump is a current steering, with Up and Down currents I_{Up}=173 μA and I_{down}=178 μA, with a detector gain constant K_ϕ=175 μA/2π rad. This circuit avoids the conventional problem in charge pumps, that limits the opening and closing of current sources, in fact, in spite of

being switched, the current is routing from the load, to a alternative path, and from that path to the load.

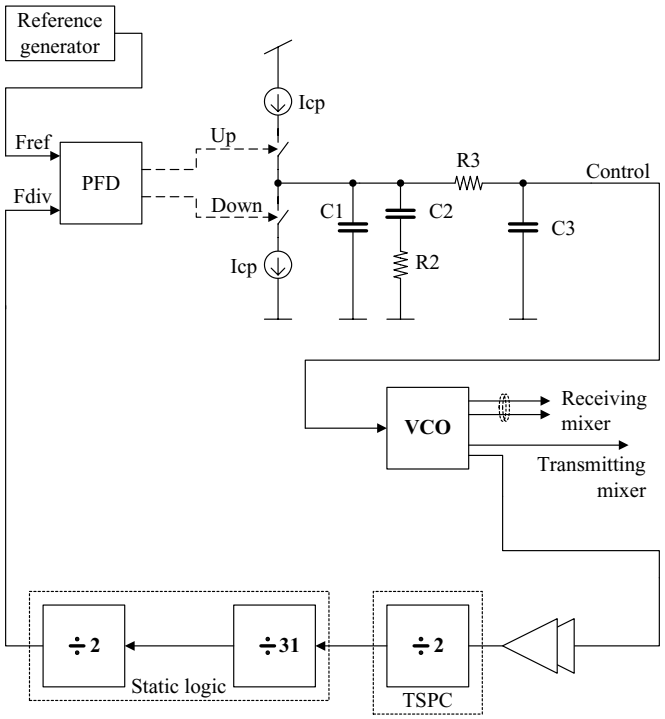

Fig. 3. PLL structure.

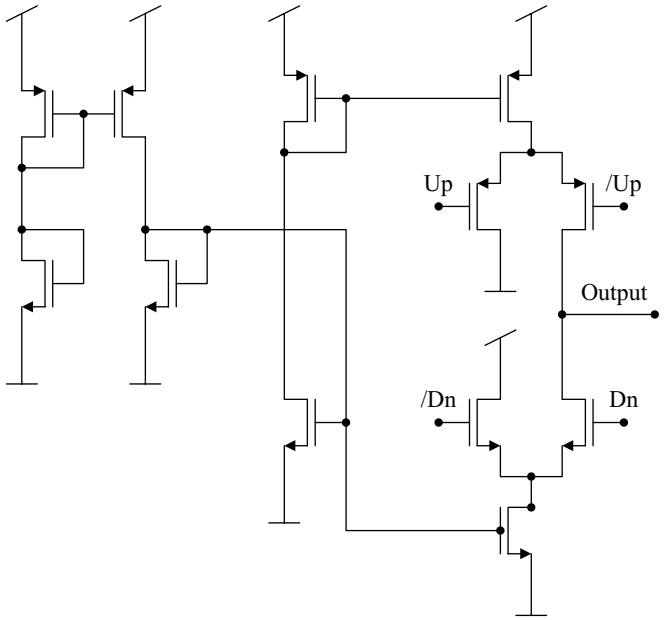

Fig. 4. Charge pump

D. Voltage controlled oscillator

A current starved ring oscillator was used as VCO [3]. This circuit has the advantage of on-chip area saving, compared with tuned LC oscillators. The inverter stage has differential outputs to be connected to the receiving mixer, while other output is reserved to the connection to a single-ended fashion to the transmitting mixer. The fourth VCO output is used to close the PLL path across the frequency divider. This VCO has the advantage to control the full range [0-1.8 V], providing a frequency range of [2.016-2.757 GHz], with a tuning constant K_{VCO}=876.6 MHz/V, calculated in the linear working range. The structure of this VCO is shown in Fig. 6.

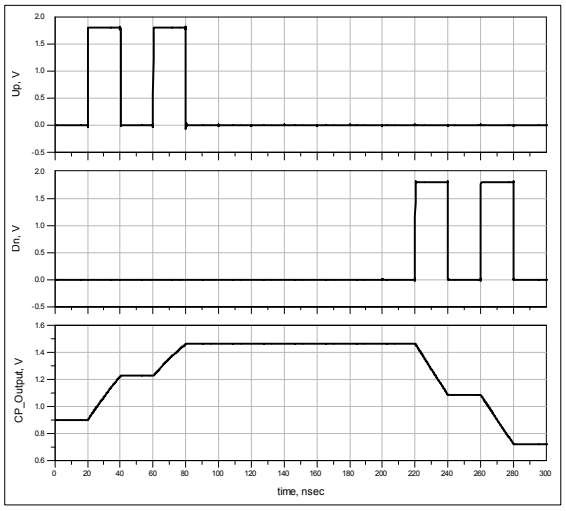

Fig. 5. V_{out} voltage, with CP connected to a capacitor C=10 μF and the V_{Up} and V_{Down} voltages.

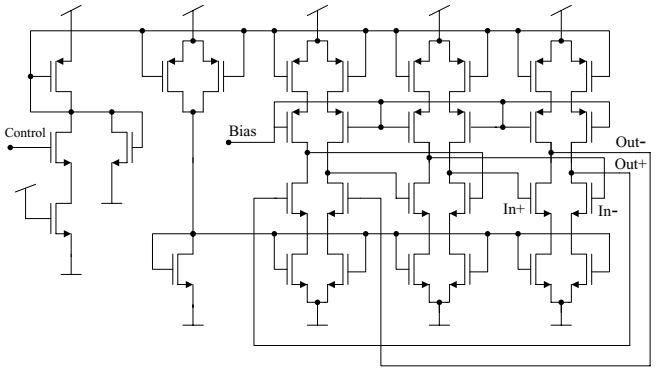

Fig. 6. Voltage controlled oscillator [3].

E. Frequency divider

The 2.48 GHz frequency is achieved with a 20 MHz reference, dividing it by 124. This is done with a cascade constituted by one half divider implemented with true single phase clock (TSPC) logic [4], one divider by 31, followed by a toggle flip-flop to enchure a duty-cycle of 50% at the PFD input (124=2×31×2). The TSPC logic was used to overcome the impossibility to implement the first toggle flip-flop with static logic in this technology. It is required a rail-to-rail supply to work properly, as depicted in Fig. 7.

The ratio of 31 was achieved with the use of frequency dividers by 2/3 with modulus control.

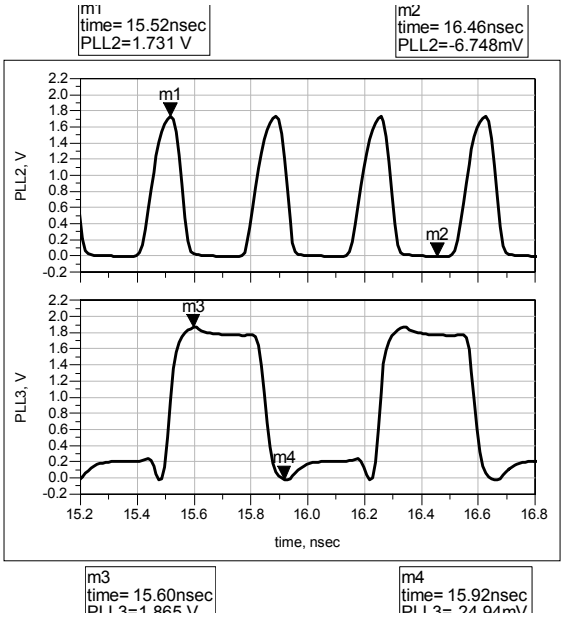

Fig. 7. Signals at the TSPC divider.

The way how division by 31 is made, depends on the modulus status across the several stages of the divider at different clock pulses. As illustrated in Fig. 8, each modulus is cleary scheduled in order to put each stage dividing by 2 or 3. At shading zones, it must be guaranty the respective modulus at zero state, to have a frequency division by 3.

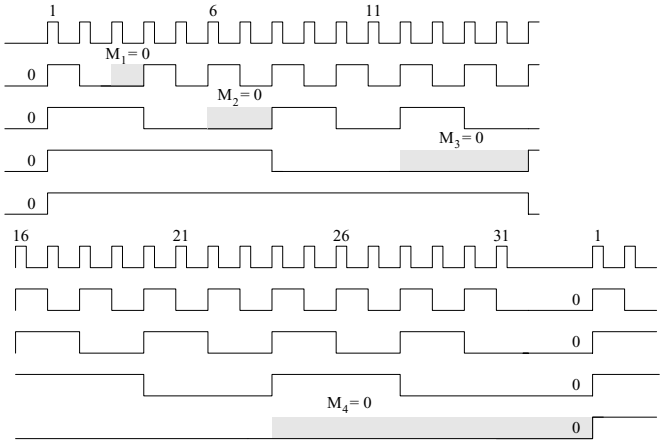

Fig. 8. Timing diagram in the divider by 31.

F. Loop filter

Ring oscillators have more phase noise than LC oscillators. For overcoming this limitation, the bandwidth of the PLL must be high enough to "clean-up" the output spectrum around 2.4 GHz. A third order passive filter, composed by a second order section (C_1, C_2 and R_2) and a first order section (C_3 and R_3), providing an additional pole it is used. The first order filter reduces spurs caused by the multiples of the reference frequency, which consequence is the increasing of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL bandwidth and below the reference [5]. A bandwidth of approximately two times the difference of the maximum and minimum frequencies generated by the VCO were used. The stability in the loop was obtained with a phase margin of 45º.

G. Transmitting and receiving mixers

It is enough to achieve a bit error probability less that 10^{-6} with a sensibility of -75 dBm, in a transmitted power of 0 dBm using ASK modulation.

Frequency upconversion is made with only one transistor directly connected to a class E power amplifier.

Downconversion used a double-balanced switched transconductor mixer [6]. The advantage is that the switching stage is directly connected to the power rails, requiring a less voltage headroom. This simplifies the switching process and has a slightly bigger conversion gain. Moreover, this topology also eliminates the presence of the strong carrier at the output, producing only odd harmonics of the local oscillation frequency.

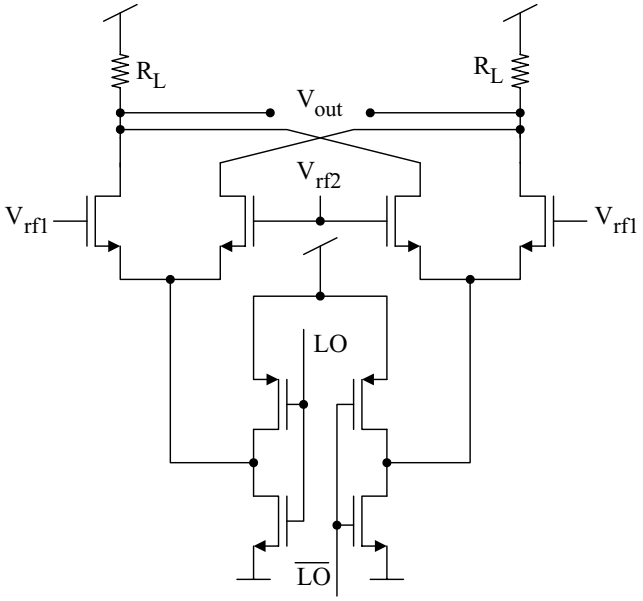

Fig. 9. Receiving mixer [6].

III. APPLICATIONS

This transceiver is being projected and optimised for low-power short-range applications. A possible application is its integration into everyday clothing, for monitoring biomedical data, during wake and sleep-time, providing clinical and prognostic significance data [7]. This data can be transmitted toward a base-station for further processing and analysis.

IV. CONCLUSIONS

A low-power low-voltage radio-frequency transceiver at 2.4 GHz, working with a supply voltage of 1.8 V was

presented in this paper. Simulations shown a power consummation less than 10 mW for the receiver. Innovative techniques were included in the frequency divider, e.g., the use of TSPC logic. This logic can overcome the limitation of this technology to toggle in static logic, signals at frequencies above 2 GHz. The receiving mixer was designed, with a new switched transconductance technique. This RF CMOS transceiver will be applied in a wireless electronic shirt for helping health professionals with rapid, accurate and sophisticated diagnostic concerning cardiopulmonary disease in order to evaluate the presence of breathing disorders in free-living patients.

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