Novel Very Small Dual-Band Chip-Size Antenna for Wireless Sensor Networks

P. M. Mendes¹, M. Bartek², J. N. Burghartz², J. H. Correia¹

¹Dept. of Industrial Electronics, University of Minho, Portugal Tel.: +351-253510382, Fax: +351-253-510189, e-mail: paulo.mendes@dei.uminho.pt ²Lab. of High-Frequency Technology and Components/ DIMES Delft University of Technology, the Netherlands

Abstract - We report on the design of a novel, very small dualband antenna having double-folded structure and suitable for onchip integration in wireless sensor network nodes. The antenna operates simultaneously at 2.4 GHz and 5.7 GHz with a -10 dB return-loss bandwidth of 50 MHz and 170 MHz, respectively. A prototype fabricated on a 4003 RogersTM substrate (dielectric permittivity of 3.38) has dimensions of 6x8.5 mm².

Index Terms – Microstrip antenna, dual-band, integrated antenna, sensor network.

I. INTRODUCTION

Wireless sensor networks are an emerging technology that brings not only numerous opportunities but also many technological challenges [1]. There are various physical quantities in different environments that when measured and recorded, could bring new quality to our lives. If e.g. soil properties like humidity, temperature, chemical composition, etc. could be measured in a distributed way, providing detailed local data for an entire farm field, the watering and nutrition supply could be adapted locally resulting in optimum growing conditions and thus significant savings.

To be effective and to have the ability to adapt itself to complex environments, like a farm field or an office building, each sensor node has to be autonomous. This means that, desirably, it should be self-powered and provided with wireless communications. This type of systems usually requires low power consumption (battery life-time) and uses low data-rate communications (small bandwidth) and, therefore, requiring special design [2].

Application of such distributed sensing systems will be highly facilitated if cheap and easy-to-use 'on-chip' or 'inpackage' solutions, equipped with short-range wireless communication capabilities, would be available. Potential merging of antenna and circuitry has led to innovative RF front-end designs with several desirable features such as compactness, lower power consumption, and added design flexibility [3]. The necessary on-chip integrated transceivers, from baseband to antenna input/output, are already available. However, the antenna, as the key element in achieving a fully integrated solution, notwithstanding all the development efforts, still remains to be an open challenge. Full integration requires the availability of very-small antennas that can be fitted into a single chip. Here, short-range wireless communication systems operating in the 5-6 GHz ISM band may play an important role due to the possibility of smaller antennas, as the antenna size is wavelength dependent.

Several small and planar antenna types have been proposed for wireless communications [4] but none of them was designed to fulfill all the restrictions and requirements set by on-chip integration. Those restrictions include the properties of available substrate materials and the way they can be processed. Many of the previously proposed solutions to integrate antennas on-chip have been based on the design of planar antennas using silicon as substrate. Since the lowohmic silicon substrate suffers from high losses, highresistivity silicon or bulk micromachining have to be used in order to increase the antenna efficiency. An optional solution to decrease the antenna losses is to use a combination of a low-loss material with silicon. The new material can be used as antenna substrate and as a carrier for required high-quality passives [5]. The silicon will be used to implement the necessary circuitry.

Such combination of substrates can be achieved with the use of wafer-level packaging (WLP) techniques, like adhesive wafer bonding and through-wafer electrical via formation, which allows combination of silicon together with different silicon-compatible substrates [6]. The typical siliconcompatible substrates (e.g. glass, BCB, polyimide, SU-8) have lower dielectric constant compared to silicon. In this way, the use of such materials reduces the losses at the expense of a size increase of the integrated antenna. Therefore, the use of an advanced antenna design may be required to overcome this drawback, providing a small and effective radiator.

Full integration requires availability of very-small antennas that can be fitted on a single chip. In our previous work [7] and work of other groups [8], the use of shorted-folded patch antennas was considered. Though the achieved results are promising, the dimensions of the developed antennas are still rather large. In this work, we demonstrate that double-folded structure based on multiple-stacked substrates achievable using WLP techniques results in further antenna-size reduction with the added benefit of dual-band operation. An antenna operating at two different ISM bands will be presented.

II. ANTENNA DESIGN

Fig. 1 shows the proposed double-folded patch antenna. The antenna is formed by four horizontal metal sheets that are electrically connected by two vertical metal walls. In practical realization, the walls can be formed by metallized via fences or slots. All this is embedded in a dielectric substrate having certain electrical permittivity and dielectric losses. These two parameters together with the antenna geometry, and its effective dimensions, will determine the radiation characteristics and the overall performance. To obtain high efficiency, the metal layers should have minimum losses and the substrate material used (silicon-compatible to allow onchip antenna integration) should be as low-loss as possible.



Fig. 1. Model of the proposed double-folded patch antenna.

A folded patch antenna was first designed to operate at 2.4 GHz by simulation performed with a high frequency structure simulator (HFSS) software. This simulation tool was already used previously for antenna design, where good match between modeling and experimental results was achieved. As it is well known, in a patch antenna, its electrical patch length determines the operating frequency. In a folded patch, the operating frequency can also be adjusted with the proper selection of the middle patch length or changing the substrate thickness. Folding the antenna structure once more offers new design possibilities. It can be used to design a smaller antenna or to obtain an antenna operating simultaneously inside two ISM bands, 2.4 GHz and 5.7 GHz. The operating frequencies can be controlled by the substrates thickness, by the gap

between the embedded patches and vertical walls, and, of course, by the overall antenna dimensions.

III. ANTENNA FABRICATION

Fig. 2 shows the prototype built on a triple stack of 4003 RogersTM substrates and designed to operate simultaneously at the 2.4 GHz and 5.7 GHz ISM bands.



Fig. 2. Photograph of the proposed and fabricated prototype of a double-folded patch antenna. The antenna lateral dimensions are $11x11 \text{ mm}^2$ and the total thickness of the triple substrate stack is 4.5 mm.

The designed antenna was fabricated on a stack of three 4003 RogersTM substrates since this substrate has electrical properties (dielectric permittivity and losses) similar to some silicon-compatible materials. In this way, it is possible to have a better idea of the expected properties of an integrated antenna fabricated with the silicon-compatible materials.

The antenna fabrication started with the drilling of the shorting and feeding vias. This was done using a standard PCB drilling machine. This machine was used to make holes that are 700 μ m in diameter. After that, the drilling machine was also used to remove the undesired copper foil in order to obtain the desired antenna geometry (define the embedded patches dimensions). The bottom and top antenna parts where then obtained by dicing using a PCB cutting machine. The feeding and shorting vias were created and both substrates placed together. Finally, a strip of copper tape was used to realize the wall interconnecting the ground plane and the second embedded patch.

The on-chip antenna integration can be achieved by means of wafer level packaging, as discussed in [6] for a folded-patch antenna. All the S-parameter measurements were performed with a vector network analyzer previously calibrated using one-port calibration.

As mentioned previously, the antenna concept based on double folding not only reduces the antenna lateral dimensions but also provides new degrees of design freedom. Folding makes the electrical path longer and the antenna operating frequency is shifted down. Fig. 3 shows the effect of double folding of the patch antenna. Since the electrical length is increased the original resonance at 2.4 GHz (single-folded antenna) moves down to 1.55 GHz and, next to that, a new resonant point at 4.48 GHz will appear. The drawback when the operating frequency shifts down is as a small reduction in the efficiency from 92% to 90%. The bandwidth is also slightly reduced. However, this is not a problem in sensor applications, where low data-rates communications are expected.



Fig. 3. Comparison of simulated and measured double-folded patch antenna return loss data.

Fig. 3 also shows a comparison between the simulated and the measured data. It can be observed that the measured and simulated operating frequencies are slightly shifted. This can be explained by the inaccuracies introduced during the fabrication steps, mainly the use of copper tape to interconnect the ground plane and the second topmost patch. A small shift in the position of this shorting wall will introduce a shift in the gap between the embedded patch and this shorting wall. This gap is a parameter that controls the antenna operating frequency.

From Fig. 3 it can also be observed that the match obtained at the higher frequency is lower then the match at the lower frequency. This is not a problem, because it is possible to use the feeding position to adjust the match at both frequencies. To verify that, the model used to design the prototype of Fig. 2 was then used to design and match an antenna operating inside two ISM bands of interest. The new antenna was designed to operate simultaneously at 2.4 GHz and at 5.7 GHz. The obtained simulated results are shown in Fig. 4. It can be observed that the return loss at the operating frequencies is now similar. The matching was increased at the higher frequency by the reduction of the matching at the lower frequency.



Fig. 4. Antenna return loss simulation demonstrating simultaneous operation at 2.4 GHz and 5.7 GHz.

To obtain an antenna operating at the desired frequencies, it was necessary to reduce the electrical length. This can be easily achieved by the reduction of the overall antenna dimensions. To have the antenna operating as displayed in Fig. 4, the antenna dimensions were reduced to 6 x 8.5 mm². Changing the antenna dimensions introduces mismatch between the feeding line (a 50 Ω coaxial line) and the feeding point. To obtain a good match for both operating frequencies, the feeding point was shifted. It was possible to obtain a match close to -20 dB, and the -10 dB return-loss bandwidth was 50 MHz and 170 MHz for 2.4 GHz and 5.7 GHz, respectively.

The radiation diagram and gain of the obtained antenna were also investigated for the frequencies of interest. Fig. 5a and Fig. 5b display the simulated 3D radiation diagram for both operating frequencies.

At both frequencies, the radiation is mainly being directed from the aperture direction, which is the radiating element of this antenna. The simulated radiation efficiency for 2.4 GHz is \sim 91%, the efficiency for 5.7 GHz is \sim 93%.

A reduction of \sim 6 dB in the antenna gain can be observed when the frequency shifts from 5.7 GHz to 2.4 GHz. This can be explained by the electrical size of the antenna. At 2.4 GHz the antenna is electrically smaller then at 5.7 GHz. As it goes smaller, the radiation tends to be omnidirectional. And if the radiation goes all around, the directivity as well the gain becomes smaller. Concerning the reduction in the bandwidth, this gain reduction may be understood as a benefit. If we have a wireless microsystem that is moving as being used, and if it is necessary to continuously transmit information, the antenna should have the ability to radiate in all directions. That means that an antenna with low gain should be used.







Fig. 5. Simulated 3D radiation pattern of the antenna operating at (a) 2.4 GHz, and (b) 5.7 GHz.

V. CONCLUSIONS

This work demonstrates a new very small antenna with dual-band operation at two different ISM bands (2.4 GHz and 5.7 GHZ). This antenna offers potential for on-chip integration, due to its small dimensions. This is a new option for antenna size reduction and a new step towards antenna integration in applications such as wireless sensor networks.

ACKNOWLEDGMENTS

The authors wish to acknowledge the support by the Portuguese Foundation for Science and Technology (SFRH/BD/4717/ 2001, POCTI / ESE / 38468 / 2001, FEDER).

REFERENCES

- Chee-Yee Chong, Srikanta P. Kumar, "Sensor Netwoks: Evolution, Opportunities, and Challenges," Proc. IEEE, vol. 91, pp. 1247-1256, 2003.
- [2] Kwyro Lee, "MICROS: an experimental coin-sized, low cost, low power CMOS zigbee-like radio at 2.4 GHz as an ubiquitous network node," in *Proc.* 24th International Conference on Microelectronics (MIEL 2004), Vol. 2, Serbia and Montenegro, 16-19 May, 2004, pp. 531-534.
- [3] K.M.K.H. Leong, T. Itoh, "Integration of electronics and antennas," in *Proc. IEEE Antennas and Propagation Soc. Int. Symp.*, vol. 2, June 2003, pp. 647 - 650.
- [4] Kin-Lu Wong, Planar Antennas for Wireless Communications, John Wiley & Sons, Inc., 2003.
- [5] P.M. Mendes, S. M. Sinaga, A. Polyakov, M. Bartek, J.N. Burghartz, J. H. Correia, "Wafer-Level Integration of On-Chip Antennas and RF Passives Using High-Resistivity Polysilicon Substrate Technology", *In Proc.* 54th ECTC, Las Vegas, USA, 2004, pp. 1879 – 1884.
- [6] P.M. Mendes, A. Polyakov, M. Bartek, J.N. Burghartz, J. H. Correia, "Folded-Patch Chip-Size Antennas for Wireless Microsystems using Wafer-Level Chip-Scale Packaging," *in Proc.* MME 2003, Delft, Netherlands pp. 77-80.
- [7] P. M. Mendes, A. Polyakov, M. Bartek, J. N. Burghartz, J. H. Correia, "Integrated 5.7 GHz Chip-Size Antenna for Wireless Sensor Networks," *Transducers* '03, Boston, USA, June 8-12, 2003, pp. 49-52.
- [8] RongLin Li; G. DeJean, M.M. Tentzeris, J. Laskar, "Development and analysis of a folded shorted-patch antenna with reduced size," *IEEE Trans. Antennas Propagat.*, vol. 52, pp. 555-562, Feb. 2004.