Spiral Inductors on Silicon for Wireless Communications

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Abstract – This paper presents the design and fabrication of integrated micromachined inductors on silicon substrates. In order to reduce eddy currents in silicon substrates, bulk-micromachining technology is used to etch the silicon wafer. In this way, aluminum spiral micromachined inductors can achieve a Q of aproximately 30 (0.6-2 nH @ 2-15 GHz). Also, the resistivity of the inductors material is discussed.

Introduction

The absence of very good inductors is a major drawback in a standard integrated circuit (IC) process. High-performance spiral inductors are the key components for the implementation of critical radio-frequency (RF) building blocks such as RF low-noise amplifiers (LNAs), voltage controlled oscillators (VCOs), low-loss impedance matching networks, passive filters, inductive loads for power amplifiers (PAs), baluns, transformers and LC tuned amplifiers. Although active circuits can be used to simulate the behaviour of an inductor, they always present greater noise, distortion and power consumption when compared to a passive inductor [2]. Critical parameters include inductance value, quality factor (Q), and self-resonant frequency (f_{SR}).

The low-ohmic silicon substrates can be used to develop spiral inductors. However, this type of silicon substrates suffers from the inherent problem of losses caused by eddy currents through the bulk substrate. An alternative solution is the use of high-resistivity substrates (HRS). Nevertheless, this kind of substrate is very expensive to build integrated CMOS circuits. In this way, silicon micromachined structures may become the solution to these RF devices.

By etching the bulk substrate, silicon micromachined inductors can be built using IC-compatible materials allowing their integration in a silicon chip, side-by-side with semiconductor circuits. Moreover, micromachined inductors would permit better front-end analog-frequency filtering than present-day filters improving power, sensitivity and reducing the physical size. In order to achieve such features, in this paper the silicon substrate is etched using micromachining techniques (wet bulk-micromachining in a KOH aqueous solution).

Aluminum is the standard material used to fabricate the metallization layers of integrated CMOS circuits and, as well, inductors because it is compatible with the silicon standard processing-steps. Another interesting material to be used for the fabrication of inductors is copper because of its lower resistivity, when compared to aluminum, leading to higher quality factors. The copper resistivity is 0.0179 Ω mm^2/m (20ºC), while the resistivity of the aluminum is 0.028 Ω mm^2/m (20ºC). However, the use of copper is not straightforward since it requires particular technology to obtain its deposition on silicon substrates.

Design and Circuit Implementation of Spiral Inductors on Silicon

The planar spiral inductor is the most implemented inductor on-chip as it can easily be built on silicon substrates [1, 2]. Such inductor can be built in IC processes, where at least two metal layers need to be used in order to form the main coil and an underpass contact that allows to reach the inner terminal of the inductance (see Fig. 1).

From the many possible geometrical configurations, the most used is the square topology (see Fig. 1) because of its easiness for design and layout fabrication [2]. The approximate inductance value for a spiral square topology can be obtained by the following expression [2]:

$$L \approx \frac{37.5\mu_0 n^2 a^2}{22r - 14a}. \quad (1)$$

where *a* is the distance between the center of the spiral and the center of the coil in *meters*, *n* is the number of turns of the coil, *r* is the radius of the spiral in *meters* and μ_0 is the permeability of the air. With this expression, the error of the approximation is smaller than 5% [2].

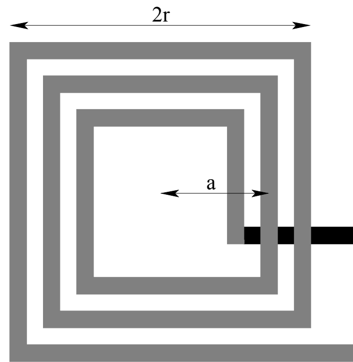

Fig. 1 – A plan view of a square spiral inductor.

The major problem of on-chip inductors is the huge die area that is consumed, even for low values of inductance. A possible model of an on-chip inductor is presented in Fig. 2. It can be seen from this model that, together with an ideal inductor *L*, there is a series resistance, R_S, which represents the ohmic losses of the metal coil as well the skin effect, and a capacitance, C_P, between the terminal wires of the inductor [1, 2]. Also, since the inductor is placed on a low-ohmic silicon substrate, the capacitances C_{ox}, C_{SUB} and the resistance R_{SUB} must be added to the model. The capacitance between the main coil and the silicon substrate, C_{ox}, is caused, mostly, by the small distance between both. The substrate resistance, R_{SUB}, represents the current flow to the substrate through C_{ox}. The capacitance C_{SUB} represents the reactive aspects inherent to the substrate [1, 2].

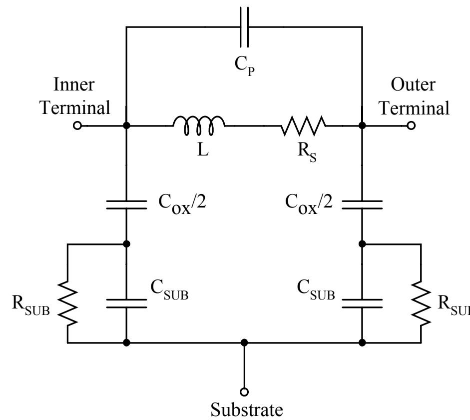

Fig. 2 – Model of an on-chip inductor in a silicon substrate.

The typical resistivity of the substrates in BiCMOS processes is 10 Ω-cm and in standard CMOS processes is less than 0.01 Ω-cm [1, 4]. Special attention is required for the standard CMOS processes because the values of the eddy currents can be significant, lowering the inductance value that was designed [2].

In order to increase the quality factor, improve the inductance value and the self-resonant frequency, the capacitance values of the model (C_{ox}, C_P and C_{SUB}) must be minimized, as well as the series resistance (R_S) and the value of the substrate resistance (R_{SUB}) increased. Several design strategies have been developed and studied to minimize the losses of an on-chip inductor such as: to design and build vertical stacked inductors [1], to avoid the lowest level metal layers in a particular process [1, 2], to minimize the doping concentration of the lossy substrate [1], to remove the inner turns of the main coil because they have minimal effect on the total magnetic flux of an inductor [2], to place a standard interrupted metal shield (or ground shield), to eliminate the eddy currents and noise coupling of the substrate [2, 3].

Our strategy will consist in removing the silicon substrate in order to increase the substrate resistance (R_{SUB}), lowering the oxide capacitance (C_{ox}) and the substrate capacitances (C_{SUB}). These improvements can reduce by far the flow of eddy currents to the lossy substrate and to increase the self-resonant frequency (f_{SR}), which will mostly depend of the interwire capacitance (C_P).

Fabrication

The bulk-micromachining technology in silicon substrate is a technology applied since the 80 years and is used to selectively remove significant amounts of silicon from a substrate.

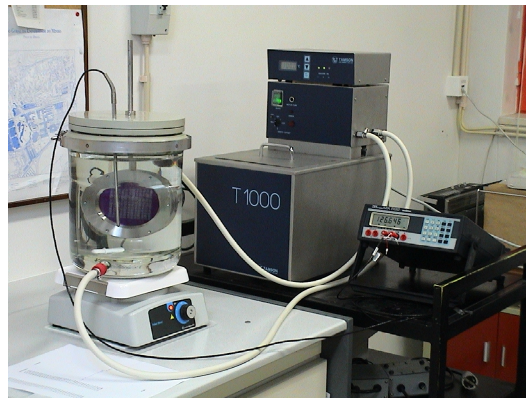

Fig. 3 – Bulk micromachining apparatus.

First, the aluminum inductors coils are created by sputtering aluminum films on the silicon wafers front-side. Then, the wafer back-side is patterned to prepare windows for anisotropic potassium hydroxide (KOH) etching. The process is done by a previously deposition of a silicon nitride membrane (or a SiO_2 layer). The membrane works as an etch-stop mask to stop the potassium hydroxide (KOH) of etching the silicon substrate.

The bulk-micromachining apparatus (see Fig. 3) is composed by an etch vessel connected to a thermostatic bath that keeps the oil temperature at 90ºC. The silicon wafer is first mounted in an O-ring holder that is suspended inside the vessel containing the KOH bath. The silicon wafer is then etched in the KOH aqueous solution (1.5 Kg of KOH per 3 liters of water). The vessel is placed on a magnetic stirrer with a magnet inside to stir the solution while etching the silicon substrate. With a temperature of the vessel KOH bath of 85ºC, the silicon etch rate is 1.4 µm per minute.

In Fig. 4 is shown the back-side of a silicon wafer etched using the mentioned before fabrication process with an aqueous KOH solution.

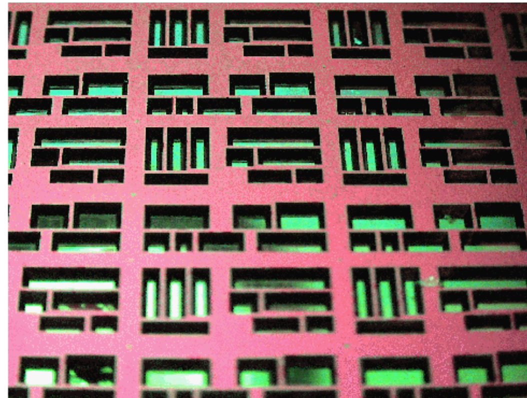

Fig. 4 – Back-side of a silicon wafer etched with an aqueous KOH solution.

Conclusions

Silicon spiral inductors were designed and its properties have been improved using bulk-micromachining technology for etching the low-ohmic silicon substrate. Due to technological constrains, aluminum was the material used to build the inductors metal layers.

In future works, the effects of the width of the strips of the inductor coil as well as the space between them is intended to be studied. Also, the use of copper for metallization layers, instead of aluminum, in collaboration with TUDelft (Delft University of Technology) is intended.

Acknowledgments

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