A 2.4-GHz wireless sensor network for smart electronic shirts integration

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***Abstract*— A typical sensing module is composed of sensors, interface electronics, a radio-frequency (RF) CMOS transceiver and an associated antenna. A 2.4-GHz RF transceiver chip was fabricated in a UMC 0.18 µm CMOS process. The receiver has a sensibility of -60 dBm and consumes 6.3 mW from a 1.8 V supply. The transmitter delivers an output power of 0 dBm with a power consumption of 11.2 mW. Innovative topics concerning efficient power management was taken into account during the design of the transceiver. A solution of individual sensing modules allows a plug-and-play solution. The target application is the integration of a wireless sensor network in smart electronic shirts, for monitoring the cardio-respiratory function and posture.**

I. INTRODUCTION

Wireless communication Microsystems with high density of nodes and simple protocol are emerging for low-data-rate distributed sensor network applications, such as those in home automation and industrial control. This type of wireless microsystem with sensors and electronics is interesting for electronic textiles as presented in this paper. Moreover, in order to implement an efficient power-consumption wireless sensor network in clothes (e.g. a electronic shirt), it was fabricated a low-power low-voltage RF CMOS transceiver.

II. RF CMOS TRANSCEIVER DESIGN

The UMC RF 0.18 µm CMOS process was used for the fabrication of a 2.4-GHz RF transceiver. This process has a poly layer and six metal layers, allowing integrated spiral inductors (with a reasonable quality factor), high resistor values (a special layer is available) and a low-power supply of 1.8 V. Therefore, a high on-chip integration is possible, in favor of better repeatability as well as lower pin count [1].

Figure 1 shows the architecture of the transceiver, which consists of a receiver, a transmitter, and a frequency synthesizer. The receiver adopts a direct demodulation through envelope detection. This is enough to achieve a bit error probability less that 10^{-6} with a sensibility of -60 dBm, for a transmitted power of 0 dBm using ASK modulation.

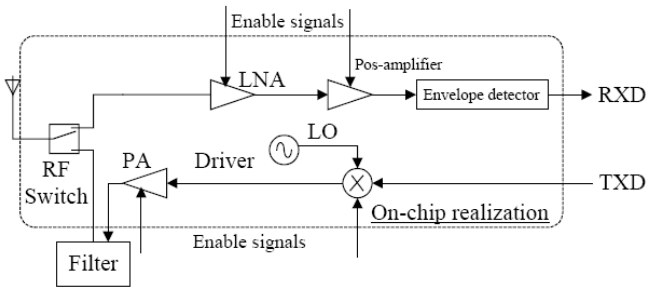

Figure 1. The block schematic of the transceiver.

Without proper design, communication would increase network power consumption significantly because listening and emitting are intensive power-consuming activities [2]. Thus, in order to optimize power consumption control signals were included in the design of the RF transceiver. With these control signals it is possible to enable and disable all the transceiver subsystems. These signals allows for example to switch off the receiver when a RF signal is being transmitted, to switch off the transmitter when a RF signal is being received, and to put the transceiver in sleeping mode when neither RF signals are being transmitted, nor being received.

A. Receiver

Figure 2 shows the receiver's front-end schematic. The low-noise amplifier (LNA) is the first gain stage in the receiver path. In a LNA, the signal must be amplified as much as possible, with a small signal-to-noise ratio (SNR) decrease. This is achieved with the best noise figure (NF). The LNA is an inductively degenerated common source amplifier [3]. This makes the input impedance at 2.4 GHz equal to 50 Ω to match with the antenna. Cascoding transistor M_2 is used to increase the gain, to better isolate the output from the input and to reduce the effect of M_1's C_{gs}. As seen in Figure 3b), the LNA is put in the sleeping mode, by

cutting the current in the polarization stage. The same principle applies to the all subsystems of the transceiver. The inductance L_s is implemented with the bonding connection to the external PCB, which has been calculated to be 0.9 nH/mm [4]. The wires used to connect the die to an external PCB, with a RF substrate, has an inductance that adds to the LNA circuit. The use of the inductance L_{sd}, helps to reduce these effects.

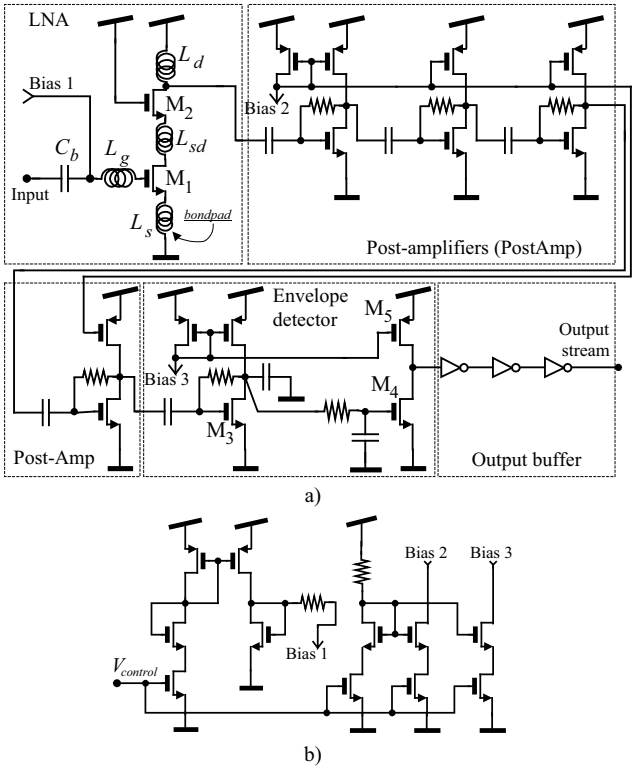

Figure 2. a) The schematics of the receiver, and b) the schematics of the bias and control circuitry of the receiver.

A minimum RF level at the envelope detector is achieved, by means of further amplification of the signal at the LNA output. This minimum level defines the receiver's sensivity. Basically, the idea of the envelope detector is as follows: an increase in the input amplifier implies a decrease in the M_3 gate voltage (this keeps the branch current constant), meaning a decrease in the M_4's gate voltage (after filtering), thus decreasing the transistor M_4 current itself. When this current reaches a point that cancels with the transistor M_5 mirror current, then the output capacitance starts to discharge and the output voltage goes to high.

B. Transmitter

The ASK modulated signal is generated by means of a switched power amplifier. The power amplifier has a cascade of five inverter, in order to drive the ASK output signal to the input of the power amplifier. Figure 3 shows the schematic of the power amplifier, as well as, the whole transmitter. The network L_1-C_1 is tuned to the carrier frequency, while the emissions outside of the 2.4 GHz band are reduced by the network L_2-C_2.

C. Frequency synthesizer

As depicted in Figure 4a), the PLL has a reference generator circuit with a crystal based oscillator at 20 MHz, followed by a phase-frequency difference circuit (PFD) without dead zone, a current steering charge pump (CP) and a third order passive filter. The passive section output is connected to the VCO, that generates the desired frequency of 2.4 GHz. This frequency must be divided by 120 and connected to the PFD again, closing the loop. In real PFDs there is an offset around the zero phase difference, and a gain inversion region takes place for phase differences higher than 2π-Δ rad. In this gain inversion region, the PFD outputs the wrong control signals increasing the phase and frequency differences between the inputs, and the lock time takes a sudden turn for the worse [5]. The implemented PFD has a linear gain in the range $-\pi$ thru $+\pi$, and a large constant gain in the range $[-2\pi, -\pi]$ and $[+\pi, +2\pi]$ [6]. This type of PFDs makes PLLs faster, compared to those using conventional PFDs.

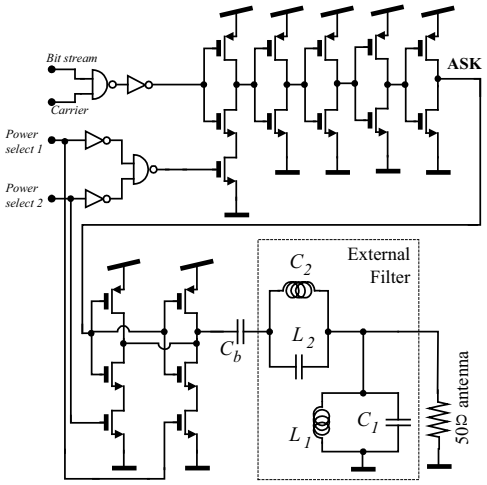

Figure 3. The schematic of the transmitter.

The charge pump (CP) is a current steering type. This circuit avoids the conventional problem in CPs, that limits the opening and closing of current sources, in fact, in spite of being switched, the current is routed from the load to an alternative path, and from that path to the load [7].

A current starved ring oscillator was used as voltage controlled oscillator (VCO). Ring oscillators have more phase noise than LC oscillators. To overcome this limitation, the bandwidth of the PLL must be high enough to *clean-up* the output spectrum around 2.4 GHz. A third order passive filter, composed by a second order section (C_1, C_2 and R_2) and a first order section (C_3 and R_3), providing an additional pole it is used. The first order filter reduces spurs caused by multiples of the reference frequency, whose consequence is the increase of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL bandwidth and below the reference. A bandwidth of approximately twice the difference between the maximum and minimum frequencies generated by the VCO was used.

The stability in the loop is obtained with a phase margin (M_ϕ) of π/4 rad [7].

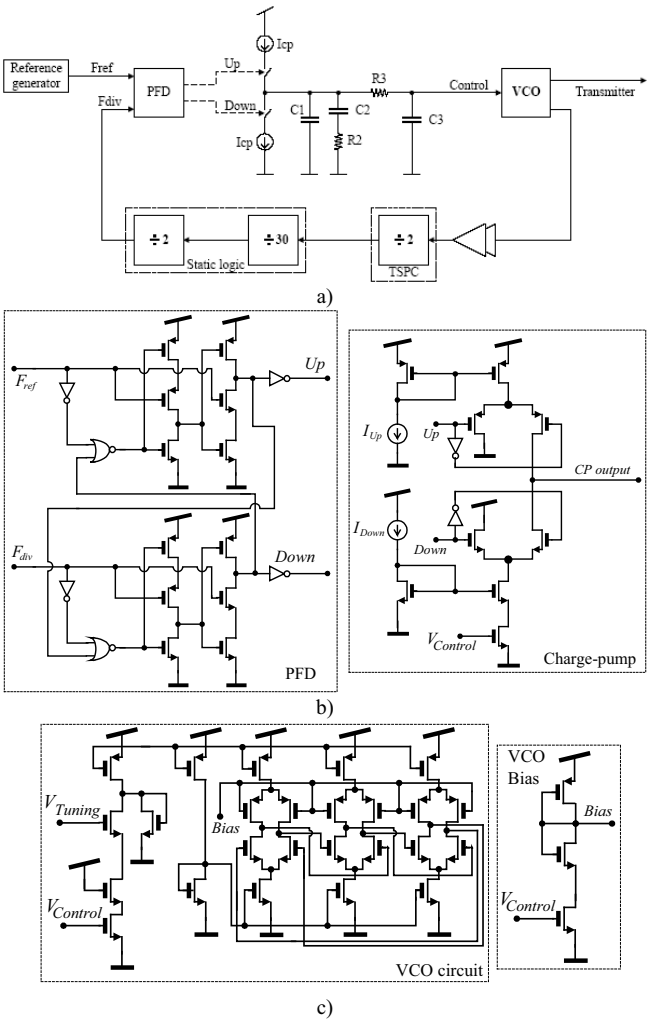

Figure 4. a) The PLL structure, b) the schematic of the PFD-CP, and c) the schematic of the VCO.

The division by 120 in the feedback path is done with a cascade constituted by one half divider, implemented with a true single phase clock (TSPC) logic [8], and one divider by 30, followed by a toggle flip-flop to ensure a duty-cycle of 50% at the PFD input. The TSPC logic was used to overcome the impossibility to implement the first toggle flip-flop with static logic in this technology. It is required a rail-to-rail input to work properly. The ratio of 30 was achieved with the use of simple frequency dividers by 2/3 with modulus control.

D. The antenna-switch

The receiver or transmitter subsystems are connected to the antenna, though a digitally controlled antenna-switch. The isolation between non-connected ports must be high to keep low the losses between connected ports. For a compact RF front-end the integration of the antenna-switch must in the same die of the transceiver [9].

III. EXPERIMENTAL RESULTS

The experimental tests made to the transceiver, shown a total power consumption of 6.3 mW for the receiver (4 mW for the LNA and 2.3 mW for the post-amplifier chain to the envelope detector), and 11.2 mW for the transmitter. The transmitter delivers a maximum output power of 1.28 mW (very close to the specified 0 dBm) with a power consumption of 11.2 mW.

The LNA has a S_{21} of 19.16 dB, a noise figure (NF) of 2.977 dB, a -1 dB compression point of -8 dBm, a -3 dB interception point of -6.4 dBm. It was noted a stabilization factor of K=1.853 (grater than the unity), that makes this amplifier unconditionally stable.

The CP has Up and Down currents of I_{Up}=173 µA and I_{Down}=178 µA, respectively, and with a detector constant gain K_ϕ=175 µA/2π rad. The used VCO has the advantage of controlling the full range [0, 1.8 V], providing a frequency range of [2.016, 2.757 GHz], with a tuning constant of K_{VCO}=876.6 MHz/V, calculated in the linear working range.

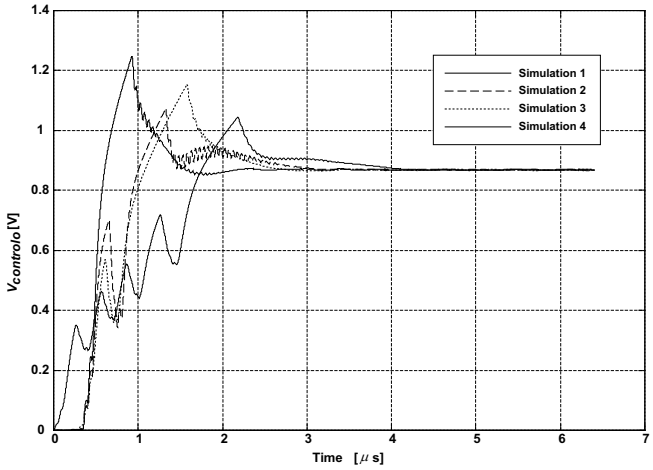

Figure 5. Behavior of the PLL's control voltage.

As shown in the figure 5, the PLL's locking times are different, according to the third-order filter. The Table I summarizes the parameters used in the simulations.

TABLE I. THIRD-ORDER FILTER LISTING.

	Filter #1	**Filter #2**	**Filter #3**	**Filter #4**
Bandwidth (kHz)	1200	1200	1200	800
M_ϕ (º)	45	55	45	45
C_1	10	11.7	18	35
C_2	81	180	185	300
R_2	5	3.7	3.5	2.7
C_3	1	1	1.5	3.5
R_3	20	20	17.5	11
Damping factor - ξ	0.755	0.858	0.809	0.787
True phase margin (º)	44.8	55.3	49.1	45.6
Lock time (µs)	1.601	2.938	2.552	10.402

The antenna-switch provides a minimum port-isolation of 41.5 dB and a maximum insertion loss of 1.3 dB, overcoming the reference values [9]. It was selected a commercial *Impexa* gigaAnt antenna, measuring 6.1 × 3.1 × 1 mm and weighting 0.05 g [10]. This antenna has a maximum return-loss of 2.5, a bandwidth of 40 MHz, an efficiency of 55%, and a nominal impedance of 50 Ω at the [2.4, 2.5 GHz] frequency range.

IV. Application

A good example for application of RF modules (embedded with the fabricated 2.4-GHz RF CMOS transceiver) is in electronic textiles where garments have not only wearable capabilities, but also have local monitoring and computational, as well as wireless communications facilities. Figure 6 shows the implementation of a wireless sensor network in a wireless electronic shirt for monitoring the cardio-respiratory function. A single channel ECG measures heart rate, a network of accelerometers records patient posture and activity level and inductive sensors are used to monitor the respiratory function.

Figure 6. A photo of the patient wearing a electronic shirt ready to plug the RF sensing module (antenna + transceiver). We can see the three connections for heart-rate with a single electrode, respiratory function and posture.

V. Conclusions

A low-power RF transceiver for a wireless EEG single-electrode module was fabricated in a UMC RF CMOS 0.18 µm process. The transceiver consumes 6.3 mW in the receive mode and delivers 0 dBm with a power consumption of 11.2 mW in the transmitting mode. These characteristics fulfill the requirements for short-range communications for using the 2.4 GHz ISM band. The main goal is to improve the medical diagnostics and therapy by using devices which reduce healthcare costs and facilitates the diagnostic while at the same time preserve the mobility and lifestyle of patients.

Figure 7 shows the photograph of the RF CMOS transceiver die, which occupies an area of 1.5 × 1.5 mm^2.

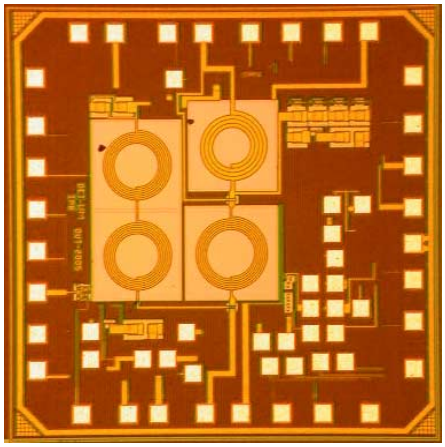

Figure 7. A die photograph of the RF CMOS transceiver.

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