FOLDED-PATCH CHIP-SIZE ANTENNAS FOR WIRELESS MICROSYSTEMS USING WAFER-LEVEL CHIP-SCALE PACKAGING

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Abstract

This paper reports on design and fabrication options of an integrated folded shorted-patch chip-size antenna for applications in short-range wireless microsystems. The antenna is built using a stack of two adhesively bonded wafers with patterned metallization and through-wafer electrical interconnects. Different fabrication options based on via formation in glass and/or high-resistivity silicon substrates using excimer laser ablation or powder blasting are analyzed.

Key words: *on-chip antenna, through-wafer vias, glass processing, laser ablation.*

I. INTRODUCTION

Wireless small-size distributed microsystems equipped with short-range communication capabilities will highly be facilitated if cheap and easy-to-use 'on-chip' or 'in-package' solutions would be available. However, a chip-size antenna, as the key element in achieving a fully integrated solution, and notwithstanding all the development efforts, still remains to be an open challenge. Together with inductances, the on-chip antenna integration can be an added benefit in order to achieve a fully integrated RF microsystem.

The antenna integration depends on the possibility to fabricate the designed structures using integrated circuits compatible materials and processes. Also, on-chip integration requires the antenna to be small and to be realised on a low-loss substrate compatible with integrated circuits operation and fabrication [1]. Patch antennas on high-resistivity silicon (HRS) or on glass are two possible options [2, 3]. Concerning the antenna efficiency, the glass substrates are superior, due to higher losses observed in HRS [3]. On the other hand, HRS has significantly higher dielectric constant than glass (11.7 vs. 5-6), so using of HRS instead of glass provides a way to reduce antenna size.

To increase the patch antenna efficiency, application of bulk-micromachining technology for selective silicon removal underneath the antenna has been proposed. However, the resulting effective dielectric constant will be lower when the silicon is removed, which leads to a larger antenna. A folded shorted-patch antenna (FSPA) can be used instead, as a compact solution for the on-chip antenna integration [4]. Due to its rather complicated structure, its implementation is not trivial.

In this paper, design and process considerations for on-chip implementation of an FSPA are presented. This antenna can be built using two-stacked glass or HRS wafers, or a combination of both. Various options for achieving antenna integration within a microsystem using wafer level chip scale packaging (WLSCP) techniques are analyzed.

II. ANTENNA DESIGN

The proposed, on-chip integrated, folded short-patch antenna is shown in Fig. 1.

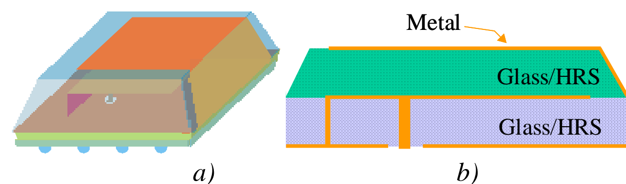


Fig. 1: Folded shorted-patch antenna: a) envisioned application; b) antenna cross-section.

It consists of three horizontal metal sheets that are electrically connected by two vertical metal walls. All this is embedded in a dielectric substrate having certain electrical permittivity and dielectric losses. These two parameters together with the antenna geometry and its actual dimensions will determine its radiation characteristics and overall performance.

For the best performance, the metal sheets should have minimum resistivity and the dielectric should be a low-loss material with high electrical permittivity. This allows achieving small antenna dimensions and high efficiency.

At frequencies above 1 GHz, glass becomes a very attractive option. Its main advantages are low losses, reasonable ε_r, availability in a form of wafers with any required thickness and diameter, and last but not least low cost.

A FSPA can be realised as a stack of two wafers with patterned metal layers and through-wafer interconnects in the form of metallized vias. High antenna efficiency requires thicker substrates (>300 µm) and therefore high aspect ratio vias in glass or HRS are required.

III. FABRICATION

Two different fabrication schemes for realization of on-chip integrated FSPAs have been proposed [5] and the antenna prototype fabrication is currently in progress. Both fabrication schemes are based on WLCSP techniques and are schematically shown in Fig. 2.

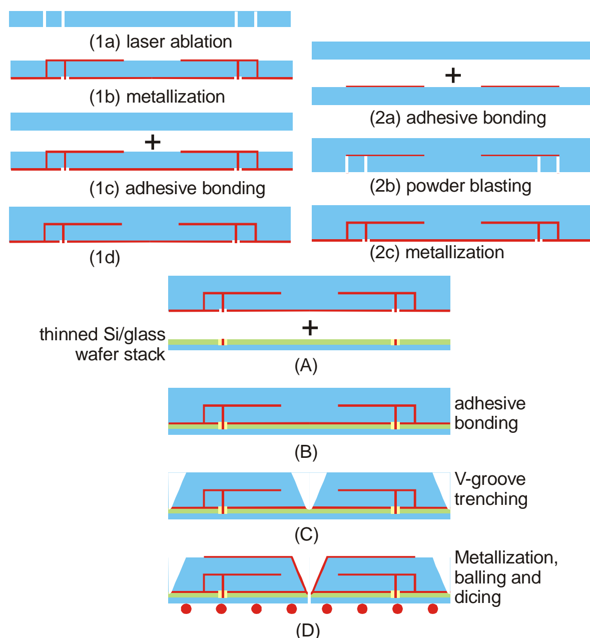
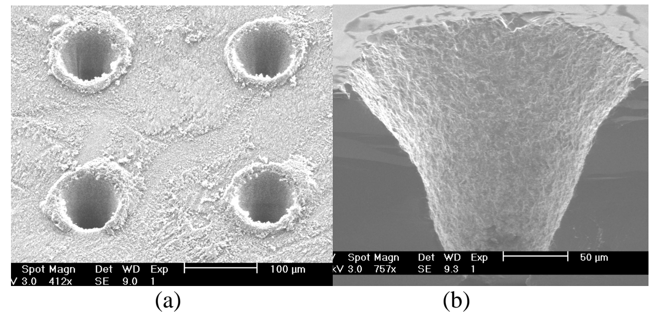


Fig. 2: Schematic fabrication sequence using laser ablated vias (left); using powder blasted vias (right).

The most demanding fabrication step required to realize the proposed antenna structure, is the through-wafer high-aspect-ratio via forming in glass. There are various techniques that can be used for via fabrication in thick glass substrates (>300 µm), but all of them have severe limitations in their throughput or achievable aspect ratios. We have explored two of them: powder blasting and laser ablation (see Fig. 3).



(a) (b)

Fig. 3: SEM picture of (a) 80 µm circular vias in a 500 µm glass substrate fabricated using a 193 nm excimer laser (front side); (b) cross-section of a 200 µm diameter powder-blasted via.

III.1. POWDER BLASTING

Powder blasting is a widely used method in glass processing. Its main disadvantage is that the typical side-wall slope is about 75° which results in rather limited achievable aspect ratio of powder-blasted vias of ~2.5:1. Fig. 3b shows a cross sectional SEM photograph of a powder-blasted, 200 µm diameter via in a 240 µm thick substrate. Higher aspect ratios are possible by applying this technique from both wafer sides.

Other interesting property of glass powder blasting, which we want to employ to simplify fabrication, is its selectivity to copper metalization.

III.2. LASER ABLATION

Glass starts to loose its transparency in the UV region and therefore excimer lasers are needed for glass ablation to form through wafer vias. Due to the limitations of the focusing system, direct ablation of the required pattern is not possible and an intermediate hard mask between the laser beam and glass wafer is required. Fig. 3a shows SEM photograph of 80 µm diameter vias formed in a 500 µm thick glass wafer using a 193 nm excimer laser. A 30:1 pattern reduction and projection optics avoid damage to the hard mask and provides high accuracy in pattern transfer.

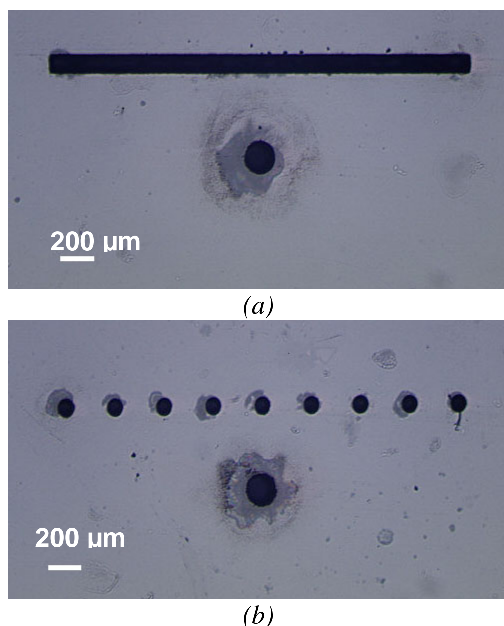
III.3. FABRICATION SCHEME

The schematic fabrication sequence is shown in Fig. 2 and has two options according the selected via-fabrication method. The first one (Fig. 2: 1a-

1d) is based on laser ablation of high-aspect-ratio vias in glass with subsequent electroless plating and patterning of the bottom and middle Cu layers, followed by glass-to-glass adhesive bonding.

The second fabrication option (Fig. 2: 2a-2c) starts with deposition and patterning of Cu layer on a glass wafer followed by adhesive bonding to the upper glass wafer (Fig. 2: 2a). The encapsulated middle Cu patch is then reached by powder blasting (Fig. 2: 2b) employing its high selectivity between copper and glass etching. This step is followed by plating and patterning of the bottom Cu layer (Fig. 2: 2c).

In both cases, the fabrication sequence continues by bonding to a pre-processed core process silicon IC wafer (Fig. 2: B) and a V-groove trenching (Fig. 2: C) using shaped dicing blade [6]. Finally the upper Cu layer is deposited and patterned. The processing sequence is completed by singulation into individual dies by dicing (Fig. 2: D).



(a)

(b)

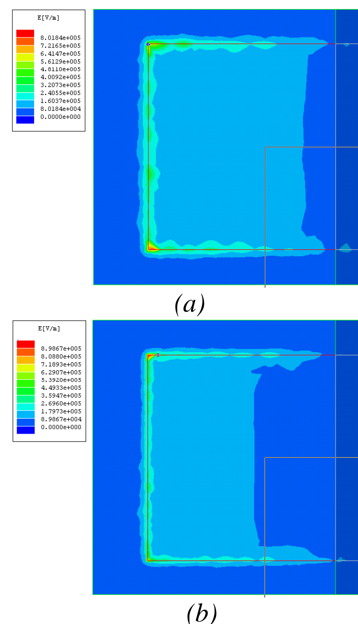
Fig. 4: Microphotograph of a 500 µm thick AF-45 glass substrate with laser ablated through-wafer vias. The antenna patch-to-ground connection is realised using (a) a 100x3000 μm^2 slit; (b) an array of 9x100 µm vias. Note that the photos are taken from the wafer back side.

Fig. 4 shows an AF-45 glass substrate from its back side after the laser ablation has been performed from the wafer front side. In Fig. 4a, the antenna patch-to-ground connection is realized as a rectangular slit of 100 x 3000 μm^2. In Fig. 4b, this connection is realized using an array of nine vias with diameter of 100 µm. As the ablation time for this type of structures is proportional to the etched area, replacing the slit with an array of vias significantly shortens the ablation time. As shown in the following section, this replacement has relatively small influence on the antenna radiation characteristics.

In case the glass substrate is replaced by HRS, the through-wafer via formation is performed using DRIE at cryogenic temperatures [7] and the overall processing becomes much easier.

IV. ANTENNA PERFORMANCE ANALYSIS

As shown in Fig. 4, and from the fabrication point of view, we have two options to interconnect the bottom ground with middle patch. We can use slits or via arrays. The electrical behavior of such options is displayed in Fig. 5.



(a)

(b)

Fig. 5: Magnitude of the electric field in the substrate: (a) antenna with vias; (b) antenna with slit.

As can been seen from electric field distribution shown in Fig. 5, the difference between these two cases is almost negligible. The same applies for the magnetic field and the surface current distribution. The conclusion that can be drawn is that both fabrication options have a very similar electrical behavior. Nevertheless, a slight adjustment of the feeding point position is necessary to achieve good impedance match.

As mentioned before, following material combinations can form the two stacked wafers: glass/glass, silicon/silicon, or glass/silicon. An option to avoid the difficult task of doing through-wafer vias in glass could be to replace the glass wafers by silicon. This will inevitably increase the dielectric losses, but at the same time the antenna dimensions could be reduced. Other option is to substitute only the bottom glass wafer by silicon. In this way, the vias in glass are not required and the overall losses are expected to be smaller.

All the proposed options were analyzed based on a FEM model built using HFSS and the results are summarized in Table 1. For various substrate options, the dimensions of the antenna model were kept constant as possible, only some minor adjustments were implemented to adjust the operating frequency and/or to achieve impedance matching.

Table 1. Summary for the different stack options.

	glass/glass (via array)	**HRS/HRS**	**HRS/glass**	**glass/glass** (slit)
F_c	5.66 GHz	5.66 GHz	5.64 GHz	5.75 GHz
BW	60 MHz	57 MHz	63 MHz	61 MHz
Eff.	66 %	47 %	60 %	69 %
L	3.2 mm	1.8 mm	3.2 mm	3.2 mm
L_1	2.6 mm	1.65 mm	2.3 mm	2.6 mm

(F_c – Operating frequency, *BW* – Bandwidth, *Eff.* - Efficiency, *L* - Top patch length, L_1 - Middle patch length)

As can be seen from Table 1, the antenna built on a stack of two glass wafers has the highest efficiency and the largest dimensions. The antenna on a stack of two HRS wafers is the smallest and has the lowest efficiency. When the glass/HRS stack is used, a compromise can be obtained. The losses are slightly increased and the dimensions don't change significantly. Table 1 compares also the glass-based antennas when slit or an array of vias is used. Similarity in their performance can be observed.

V. CONCLUSIONS

Ansoft HFSS 3-D EM simulation tool was used to design folded-patch chip-size antennas for operation in 5-6 GHz frequency range. Different fabrication options, based on wafer-level chip-scale packaging techniques, and their influence on antenna electrical performance were analysed. The glass/glass, HRS/HRS and glass/HRS substrate combinations were considered from the electrical as well as fabrication point of view. Fabrication of high-aspect-ratio vias (>5:1) in thick glass substrates (>300 μm) using excimer laser ablation was demonstrated. It was predicted that the glass/glass substrate combination would provide an antenna with the highest efficiency and still acceptable dimensions. The HRS/HRS antenna will have the smallest dimensions, but efficiency will drop ~20%, when compared to antenna built on glass. The glass/HRS antenna could be an interesting option as the complicated via fabrication in glass is avoided and the efficiency drop is less than 9 %.

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