Design of a Folded-Patch Chip-Size Antenna for Short-Range Communications

P. M. Mendes, A. Polyakov[(1)], M. Bartek[(1)], J.N. Burghartz[(1)], J.H. Correia

[(1)]Lab. of ECTM/DIMES, Delft University of Technology, the Netherlands
Dept. of Industrial Electronics, University of Minho, Portugal
Tel.: +351 253510184, Fax: +351 253510189, e-mail: paulo.mendes@dei.uminho.pt

Abstract – **We report on design of an integrated folded shorted-patch (FSP) chip-size antenna for operation at 5.7 GHz and use in short-range wireless communications. Application of wafer-level chip-scale packaging (WLCSP) techniques like adhesive wafer bonding and through-wafer electrical via formation, combined with the selected antenna type allows antenna on-chip integration. The operating characteristics of a folded S-P antenna built on two stacked glass substrates were analysed with respect to substrate thickness, middle patch length and substrate sidewall angles. Antenna size reduction down to 4x4x1 mm^3, efficiency of 66 % and bandwidth of 62 MHz are predicted.**

I. Introduction

Application of distributed systems equipped with short-range wireless communication capabilities will highly be facilitated if cheap and easy-to-use 'on-chip' or 'in-package' solutions would be available. Short-range wireless communication systems operating in the 5-6 GHz ISM band play an important role in the current communication standards. On-chip integrated transceivers, from baseband to antenna input/output, have already become technologically possible. However, the antenna, as the key element in achieving a fully integrated solution and notwithstanding all the development efforts, still remains to be an open challenge.

Several small and planar antenna types have been proposed for wireless communications [1] but none of them was designed to meet all the restrictions and requirements set by on-chip integration. Those restrictions include the properties of available substrate materials and the way they can be processed.

Previously proposed solutions for on-chip antennas integration have been based on the design of patch antennas using silicon as substrate. However, since the 'standard' silicon substrate is a lossy material, high-resistivity silicon or bulk micromachining have to be used in order to increase antenna efficiency. A different approach is to use a low loss material compatible with integrated circuit fabrication process, like glass [2]. Since typical glass substrates have lower dielectric constant, the design of small size antennas often requires the use of folded or shorted structures.

MEMS technology and wafer-level chip-scale packaging (WLCSP) techniques when applied to packaging of RF silicon ICs represent truly added value as at a limited cost 3D passive structures can be realized. Application of WLCSP techniques, like adhesive wafer bonding and through-wafer electrical via formation, allows the use of different substrates together with silicon [3]. The use of glass wafers reduces the losses at the expense of a size increase in the integrated antenna. Nevertheless, the use of an advanced antenna design may overcome this drawback, providing a small and effective radiator. In this way, the use of glass substrate enables a small on-chip antenna and RF electronics direct coupling. This offers potential of low cost, low profile and simplified assembly. We evaluate this on folded-patch chip-size antennas.

In this work, the folded short-patch antenna was adopted as a compact solution for antenna integration [4]. We have adapted the WLCSP technology of ShellCase [5] for on-chip integration of such folded-patch antenna. The envisioned application and the fabrication constraints define some critical antenna parameters that have to be optimised. In this paper, we study the influence of substrate thickness and die sidewall angles, as the main fabrication parameters, on the overall antenna characteristics.

II. Antenna Design

In our previous work, various antenna prototypes were designed to achieve antenna integration [6]. Those prototypes were based on a patch antenna design realised using high-resistivity silicon (HRS) or glass substrates. In Fig. 1, a chip-size patch-type antenna prototype fabricated on HRS is shown.

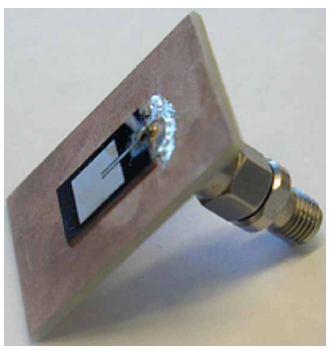

Fig. 1: Patch chip-size antenna.

Using the HRS substrate, the achieved and measured antenna efficiency (~20%) is rather low. A similar design when realised using a glass substrate, was able to provide

an antenna efficiency of around 60%. Its drawback is the significant antenna size increase.

One solution to overcome the size restriction is to use a folded structure, as shown in Fig. 2.

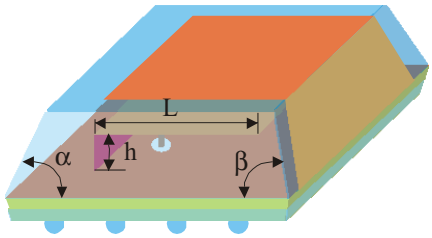

Fig. 2: Folded shorted-patch antenna.

The main drawback of this folded structure is its increased fabrication complexity. However, the advances in WLCSP techniques make its implementation feasible. Further on, various fabrication constraints of this folded structure and their influence on antenna performance will be analysed.

A Antenna Fabrication

As can be observed in Fig. 3, the proposed antenna is built using two stacked wafers. This wafer stack is obtained by wafer bonding. The feeding and the shorting connection between the metal ground and the middle metal layer are obtained with the formation of through wafer vias. To obtain a connection between the upper patch and the ground plane, it's necessary to pattern a metallic vertical wall or, preferably, an angled wall. Other possibility is to define this geometry by the dicing process. Since, for each substrate layer, one wafer has to be used, the wafer thickness defines the distance between patches and therefore dictates the overall antenna thickness (Fig. 3 -d).

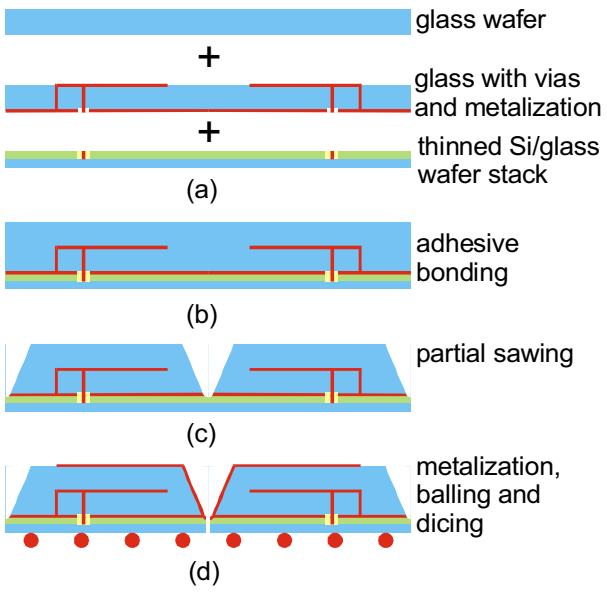

Fig. 3: Schematic fabrication sequence.

All these geometrical fabrication constrains have certain influence on the overall antenna characteristics and are the subject of the following section.

B Antenna Analysis

The antenna was designed to operate at 5.7 GHz, a frequency chosen to be inside the 5-6 GHz ISM band. The antenna model was built in HFSS 8.5 from Ansoft, where all the simulation analysis was performed. This simulation tool was intensively used previously in our patch antenna design [2], [6], where good match of modeling and experimental results was achieved.

To complete the model design, it was necessary to know the properties of the glass wafer that will be used to fabricate the prototype. Those electrical characteristics were obtained using the method described in [7]. The developed antenna model is displayed in Fig. 4.

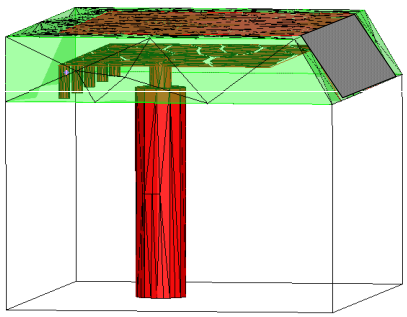

Fig. 4: HFSS model of the folded shorted-patch antenna.

As discussed before, from the fabrication point of view, slanted sidewalls are preferable instead of vertical ones. The first analysis was to investigate the effect of inclined walls when compared to vertical ones. In Fig. 5, the effect of the sidewall angles on the return loss is shown. The observed shift in the operating frequency is mainly due to the top patch size variation when the wall angle changes.

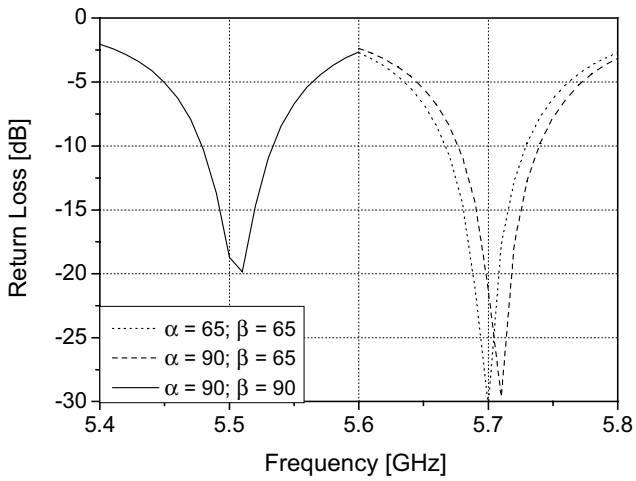

Fig. 5: Return loss of the folded S-P antenna for different sidewall angles.

Since the walls inclination could have some influence on the direction where the antenna radiates, the radiation patterns were investigated for different fabrication methods. The obtained results are displayed in Fig. 6.

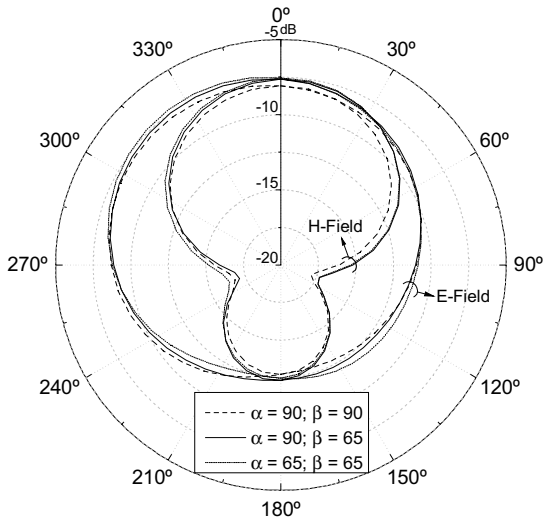

Fig. 6: Far-field co-polar patterns of the folded S-P antenna at 5.7 GHz for different sidewall angles.

It can be observed that the far-field radiation diagram remains almost the same for different sidewall angles, with maximum gain directed to ~315º.

From this analysis, the main influence when using slanted sidewalls, instead of vertical ones, will be the operating frequency shift. However, this can be compensated with a small increase in the antenna size since, in a patch antenna, the patch length determines the operating frequency. Furthermore, the operating frequency of the proposed antenna can also be adjusted by proper selection of the middle patch length, *L*. This tuning effect is observed in Fig. 7.

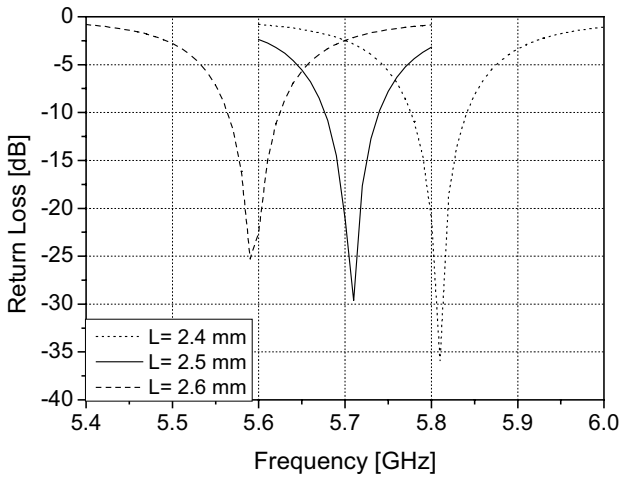

Fig. 7: Return loss of the folded S-P with different lengths for the lower patch.

In this analysis, all the antenna parameters were kept constant, except the dimension *L*. It was observed that this is an effective method that can be used to select the antenna operating frequency. The drawback is the small (~3-5 %) reduction of the antenna efficiency when the size of the middle patch is increased significantly and approaches the ground wall.

From the fabrication point of view, it is also preferable to keep the overall antenna thickness small. To achieve this, thin or thinned wafers can be used. However, the substrate thickness is one parameter that influences the antenna performance. To study this effect, all the dimensions were kept constant, except the wafer thickness, *h*, which was modified. The obtained results are presented in Fig. 8.

It can be observed that decreasing the wafer thickness leads to a reduction in the antenna operating frequency. This is a desirable effect since, for the same operating frequency, the antenna can be smaller. The drawback is the efficiency and bandwidth reduction.

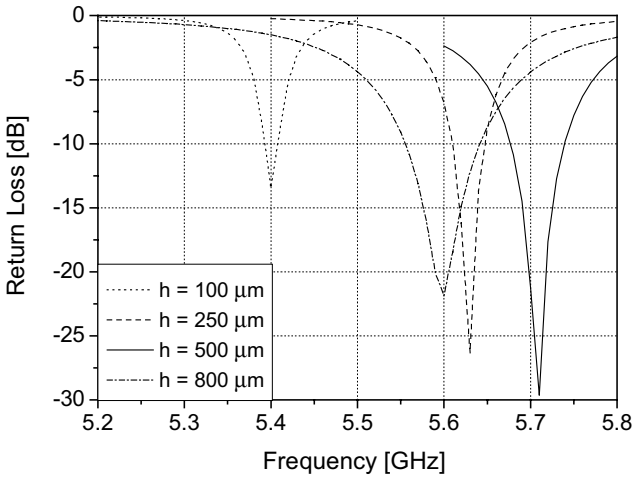

Fig. 8: Return loss of the folded S-P antenna for different substrate thickness values.

The following table summarizes the observed effects when changing the wafer thickness.

Table 1: Summary of antenna properties for different substrate thickness values.

Substrate Thickness [µm]	Frequency [GHz]	Bandwidth [MHz]	Efficiency [%]
100	5.4	17	23
250	5.63	39	48
500	5.71	62	66
800	5.6	88	76

III. CONCLUSIONS

This work demonstrates that folded-patch antennas built on glass substrates operating in the 5-6 GHz ISM band are feasible using WLSCP integration and suitable for wireless short-range links. A folded shorted-patch antenna was designed and it was shown that the main technology constraints do not have negative influence on the overall antenna characteristics.

ACKNOWLEDGEMENT

The authors wish to acknowledge the Portuguese Foundation for Science and Technology for funding this work (SFRH/BD/4717/2001 and POCTI / ESE / 38468 / 2001, FEDER).

REFERENCES

[1] Kin-Lu Wong, *Planar Antennas for Wireless Communications*, John Wiley & Sons, Inc., 2003.

[2] P.M. Mendes, M. Bartek, J.N. Burghartz, J.H. Correia, "Design and Analysis of a 6 GHz Chip Antenna on Glass Substrates for Integration with RF/Wireless Microsystems", IEEE APS Int. Symp., Columbus, Ohio, USA, June 22-27, 2003.

[3] A. Polyakov, P.M. Mendes, S.M. Sinaga, M. Bartek, B. Rejaei, J.H. Correia, J.N. Burghartz, "Processability and Electrical Characteristics of Glass Substrates for RF Wafer-Level Chip-Scale Packages", Proc. ECTC 2003, New Orleans, USA, May 27-30, 2003.

[4] R. L. Li, G. DeJean, E. Tsai, E. Tentzeris, J Laskar, "Novel Small Folded Shorted-Patch Antennas", IEEE APS Int. Symp., Vol. 4, pp. 26-29, 2002.

[5] www.shellcase.com.

[6] P. M. Mendes, A. Polyakov, M. Bartek, J. N. Burghartz, J. H. Correia, "Integrated 5.7 GHz Chip-Size Antenna for Wireless Sensor Networks", Proc. Transducers'03, Boston, USA, June 8-12, 2003, pp. 49-52.

[7] P. M. Mendes, A. Polyakov, M. Bartek, J. N. Burghartz, J. H. Correia, "Extraction of Glass-Wafers Electrical Properties Based onS-Parameters Measurements of Coplanar Waveguides", ConfTele 2003, Aveiro, Portugal, June 18-20, 2003.