Low-power 2.4-GHz RF transceiver for wireless EEG module plug-and-play

J. P. Carmo
Polytechnic Institute of Braganca
Campus Santa Apolonia
5301-854 Braganca, Portugal
jcarmo@ipb.pt

N. Dias, P. M. Mendes, C. Couto, J. H. Correia
University of Minho, Dept. Industrial Electronics
Campus Azurem
4800-058 Guimaraes, Portugal

***Abstract*—This paper presents the design and fabrication of a radio-frequency (RF) transceiver fabricated in a UMC RF 0.18 µm CMOS process. The RF transceiver was built to operate at the 2.4 GHz ISM band. The receiver has a sensibility of -60 dBm and consumes 6.3 mW from a 1.8 V supply. The transmitter delivers an output power of 0 dBm with a power consumption of 11.2 mW. The application is a wireless wearable electroencephalogram (EEG) braincap. Wireless EEG allows patients to wear the brain cap and maintain their mobility while simultaneously having their electrical brain activity monitored. A solution of an individual EEG module composed by an electrode, processing electronics and an antenna, allows a plug-and-play electrodes solution.**

I. INTRODUCTION

An emerging field is the wireless monitoring of human-body information. Body area network (BAN) comprises smart sensors able to communicate wirelessly to a base station. A wireless electroencephalogram (EEG) will provide a breakthrough in the monitoring, diagnostics and treatment of patients with neural diseases as epilepsy [1]. A wireless EEG module composed by the neural electrodes (non-invasive and distributed in a braincap), processing electronics and a RF transceiver with an associated antenna, will be an important breakthrough in EEG diagnostic (see Figure 1).

The RF transceiver (attached to an antenna) makes possible the data communication between the braincap and the external monitoring instrumentation used by health professionals. The transceiver must have low-power consumption, low-voltage supply and small-size so it can be assembled with an antenna and the EEG electrode. The modules are fed by a coin-sized battery placed in the braincap. The size-reduction achieved with these modules, make them suitable to be easily plugged and unplugged in the wireless EEG braincap according the interest of the medical doctors.

Figure 1. Classic EEG braincap with Ag/AgCl electrodes and respective wires.

II. RF CMOS TRANSCEIVER DESIGN

The UMC RF 0.18 µm CMOS process was used for the fabrication of a 2.4-GHz RF transceiver. This process has a poly layer and six metal layers, allowing integrated spiral inductors (with a reasonable quality factor), high resistor values (a special layer is available) and a low-power supply of 1.8 V. Therefore, a high on-chip integration is possible, in favour of better repeatability as well as less pin count [2].

Figure 2 shows the architecture of the transceiver, which consists of a receiver, a transmitter, and a frequency synthesizer. The receiver adopts a direct demodulation, by means of envelope detection. It is enough to achieve a bit error probability less that 10^{-6} with a sensibility of -60 dBm, in a transmitted power of 0 dBm using ASK modulation. These specifications makes the transceiver suitable to the operation in EEG environments, where the radiated power levels must be lowest.

1-4244-0395-2/06/$20.00 ©2006 IEEE.

A. Receiver

Figure 3 shows the receiver's front-end schematic. The low-noise amplifier (LNA) is the first gain stage in the receiver path. In a LNA, the signal must be amplified as much as possible, with a small signal-to-noise ratio (SNR) decrease. This is achieved with the best noise figure (NF).

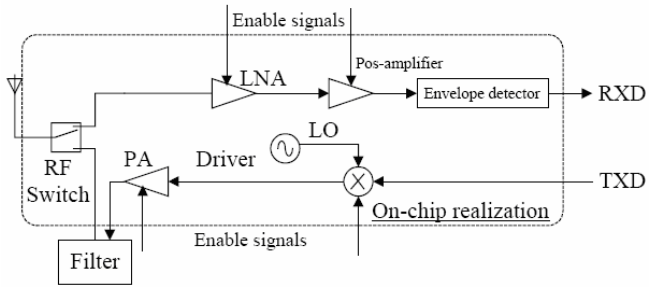

Figure 2. The block schematic of the transceiver.

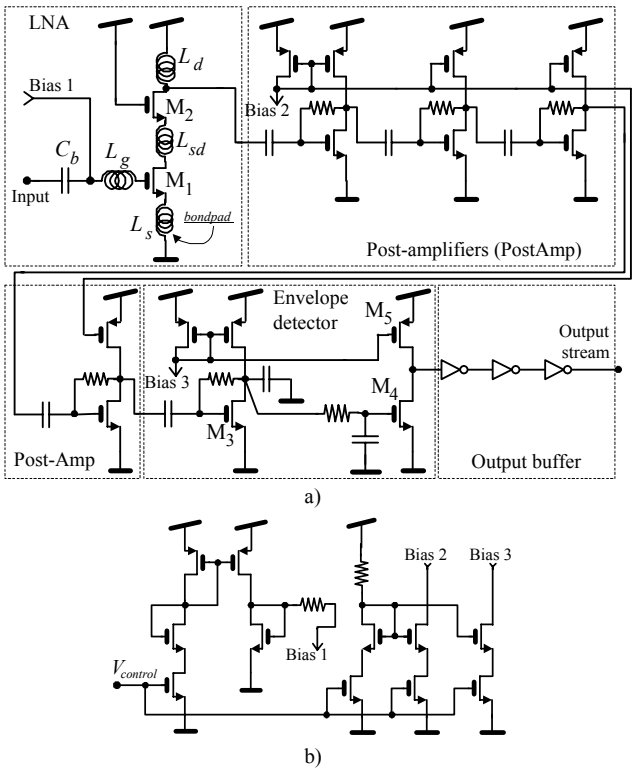

Figure 3. The schematics of the a) receiver; b) bias and control circuitry.

The LNA is an inductively degenerated common source amplifier [3]. This makes the input impedance at 2.4 GHz equal to 50 Ω, for matching with antenna-switch. Cascoding transistor M_2 is used to increase the gain, to better isolate the output from input and to reduce the effect of M_1's C_{gs}. The LNA is putted in the sleeping mode, by cutting the current in the polarization stage. The same principle applies to the all subsystems of the transceiver. The inductance L_s is implemented with the bonding connection to the external PCB, which has been calculated to be 0.9 nH/mm [4]. The wires used to connect the die to an external PCB, with a RF substrate, has an inductance that adds to the LNA circuit. The use of the inductance L_{sd}, helps to reduce these effects.

A minimum RF level at the envelope detector is achieved, by means of further amplification of the signal at the LNA output. This minimum level defines the receiver's sensibility. Basically, the idea of the envelope detector is as follows: an increasing in the input amplifier implies a decrease in the M_3 gate voltage (this keeps the branch current constant), meaning a decrease in the M_4's gate voltage (after filtering), thus decreasing the transistor M_4 current itself. When this current reaches a point that cancels with the transistor M_5 mirror current, then the output capacitance starts to discharge and the output voltage goes to high.

B. Transmitter

The ASK modulated signal is generated by means of a switched power amplifier. The power amplifier has a cascade of five inverter, in order to drive the ASK output signal to the input of the power amplifier. The Figure 4 shows the schematic of the power amplifier, as well as, the whole transmitter. The network L_1-C_1 is tuned to the carrier frequency, while the emissions outside of the 2.4 GHz band are reduced by the network L_2-C_2.

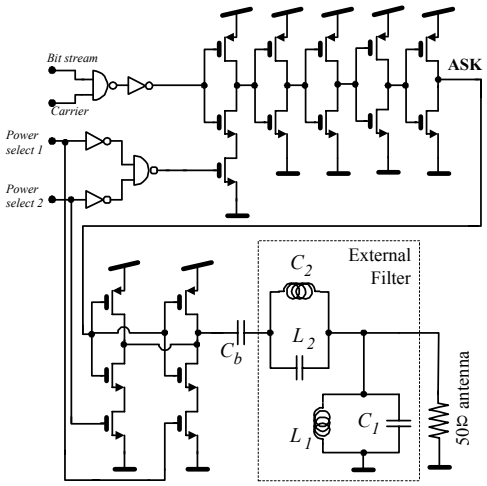

Figure 4. The schematic of the transmitter.

C. Frequency synthesizer

As depicted in Figure 5a), the PLL has a reference generator circuit with a crystal based oscillator at 20 MHz, followed by a phase-frequency difference circuit (PFD) without dead zone, a current steering charge pump (CP) and a third order passive filter. The passive section output is connected to the VCO, that generates the desired frequency of 2.4 GHz. This frequency must be divided by 120 and connected to the PFD again, closing the loop.

In real PFDs there is an offset around the zero phase difference, and a gain inversion region takes place for phase

differences higher than 2π-Δ rad. In this gain inversion region, the PFD outputs the wrong control signals increasing the phase and frequency differences between the inputs, and the lock time takes a sudden turn for the worse [5]. The implemented PFD has a linear gain in the range $-\pi$ thru $+\pi$, and a large constant gain in the range $[-2\pi, -\pi]$ and $[+\pi, +2\pi]$ [6]. This type of PFDs makes PLLs faster, compared to those using conventional PFDs.

The charge pump (CP) is a current steering type. This circuit avoids the conventional problem in CPs, that limits the opening and closing of current sources, in fact, in spite of being switched, the current is routing from the load to an alternative path, and from that path to the load.

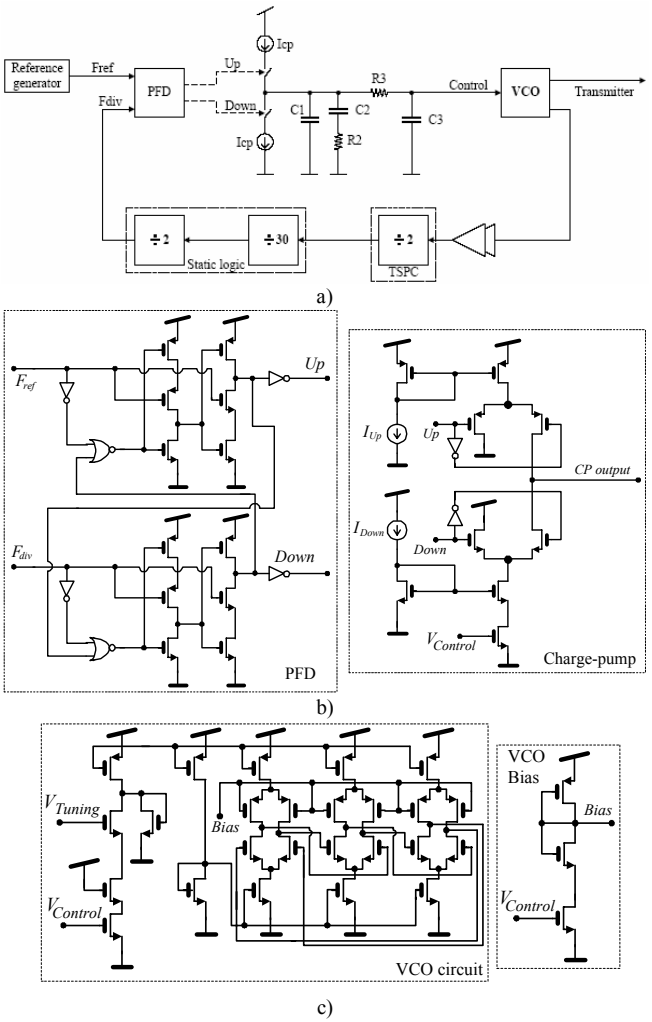

Figure 5. a) The PLL structure, b) the schematic of the PFD-CP, and c) the schematic of the VCO.

A current starved ring oscillator was used as voltage controlled oscillator (VCO). Ring oscillators have more phase noise than LC oscillators. For overcoming this limitation, the bandwidth of the PLL must be high enough to "clean-up" the output spectrum around 2.4 GHz. A third order passive filter, composed by a second order section (C_1, C_2 and R_2) and a first order section (C_3 and R_3), providing an additional pole it is used. The first order filter reduces spurs caused by the multiples of reference frequency, whose consequence is the increasing of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL bandwidth and below the reference. A bandwidth of approximately two times the difference between the maximum and minimum frequencies generated by the VCO was used. The stability in the loop is obtained with a phase margin of $\pi/4$ rad.

The division by 120 in the feedback path is done with a cascade constituted by one half divider implemented with a true single phase clock (TSPC) logic [7], one divider by 30, followed by a toggle flip-flop to ensure a duty-cycle of 50% at the PFD input. The TSPC logic was used to overcome the impossibility to implement the first toggle flip-flop with static logic in this technology. It is required a rail-to-rail input to work properly. The ratio of 30 was achieved with the use of simple frequency dividers by 2/3 with modulus control.

D. The antenna-switch

The receiver or transmitter subsystems are connected to the antenna, by means of a digitally controlled antenna-switch. The isolation between non-connected ports must be high, keeping lowest the losses between connected ports. For a compact RF front-end the integration of the antenna-switch must in the same die of the transceiver (Figure 6).

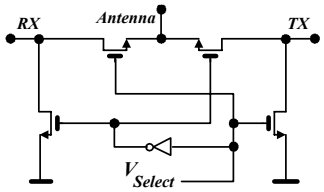

Figure 6. The antenna-switch.

III. EXPERIMENTAL RESULTS

Figure 7 shows the photograph of the RF CMOS transceiver die, which occupies an area of 1.5 × 1.5 mm^2, but the final structure can be optimized for including processing electronics for the acquired neural signals.

The experimental tests made to the transceiver, shown a total power consumption of 6.3 mW for the receiver (4 mW for the LNA and 2.3 mW for the post-amplifier chain to the envelope detector), and 11.2 mW for the transmitter. The transmitter delivers a maximum output power of 1.28 mW (very close to the specified 0 dBm) with a power consumption of 11.2 mW.

The LNA has a gain of 15.1 dB, a NF of 1.076 dB and a 1 dB compression point of -12.4 dBm. The LNA has also the stabilization factor K=1.4 (grater than the unity), that makes this amplifier unconditionally stable. The CP has Up and Down currents of I_{Up}=173 µA and I_{Down}=178 µA, respectively, and with a detector constant gain K_ϕ=175 µA/2π rad. The used VCO has the advantage to control the

full range [0, 1.8 V], providing a frequency range of [2.016, 2.757 GHz], with a tuning constant K_{VCO}=876.6 MHz/V. The observations shown a time to lock of only 2.5 µs.

The antenna-switch has a maximum NF of 1.39 dB. This antenna-switch provides a minimum port-isolation of 41.5 dB and a maximum insertion loss of 1.3 dB, overcoming the reference values [8]. It was selected a commercial *Impexa* gigaAnt antenna, measuring 6.1 × 3.1 × 1 mm and weighting 0.05 g [9]. This antenna has a maximum return-loss of 2.5, a bandwidth of 40 MHz, an efficiency of 55%, and a nominal impedance of 50 Ω at the [2.4, 2.5 GHz] frequency range.

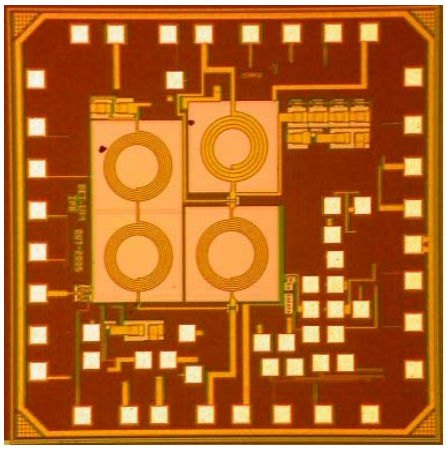

Figure 7. A die photograph of the RF CMOS transceiver.

IV. WIRELESS EEG MODULE

The standard wireless EEG solutions use a braincap with wires running from the electrodes position to a bulky central unity (amplification, signal filtering and A-to-D conversion, RF transceiver and antenna) [1]. A more interesting solution is to use compact wireless EEG modules, where the electronics, the antenna and each electrode are mounted together. The power supply for these modules is obtained locally from a coin-sized battery placed in the braincap. Also, it is possible to integrate additional electronics (amplification, filtering and high-resolution digital conversion), for local signal processing in these small-size individual wireless EEG modules.

This solution fits the medical doctor requirements for an easy placement and removal of the electrodes in the braincap. Moreover, with this solution it is very easy to populate electrodes in different positions or takeoff. In many medical diagnostics the patients are monitorized only with a low number of electrodes (e.g. 2-5 electrodes), making possible to mount an EEG wireless-electrodes network with these plug-and-play modules. Figure 8 shows a 12-mm diameter Ag/AgCl EEG electrode for mounting the complete module. The RF CMOS transceiver and associated antenna will be mounted in the back of the electrode package.

V. CONCLUSIONS

A low-power RF transceiver for a wireless EEG single-electrode module was fabricated in a UMC RF CMOS 0.18 µm process. The transceiver consumes 6.3 mW in the receive mode and delivers 0 dBm with a power consumption of 11.2 mW in the transmitting mode. These characteristics fulfill the requirements for short-range communications for using the 2.4 GHz ISM band. It was also presented, a plug-and-play EEG module composed by the fabricated RF transceiver, an associated antenna and an Ag/AgCl EEG electrode. The main goal is improving the EEG medical diagnostics and therapy by using devices which reduces healthcare costs and facilitates the diagnostic while at the same time preserving the mobility and lifestyle of patients.

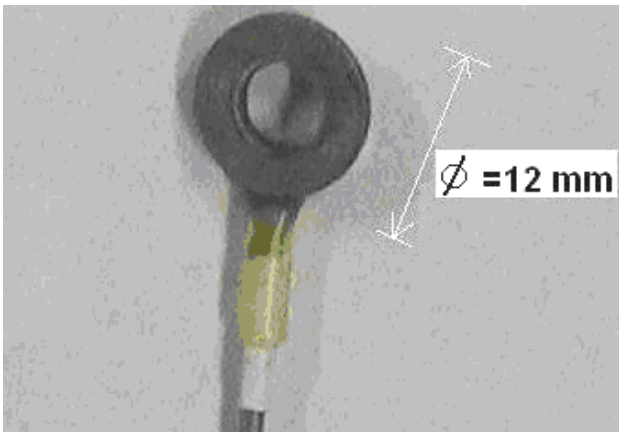

Figure 8. A photo of the EEG Ag/AgCl electrode (12 mm of diameter) that will be used to mount the antenna with the RF CMOS transceiver on its back.

REFERENCES

[1] IMEC press releases, "Ambulatory EEG", Human ++ EU project, pp. 1-2, 2003, available at IMEC's web site: http://www.imec.be/human/.

[2] P. Choi, H. C. Park, S. Kim, S. Park, I. Nam, T. W. Kim, S. Park, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, S. M. Park, K. Lee, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) applications at 2.4 GHz", IEEE Journal of Solid-State Circuits, Vol. 38, Nr. 12, pp. 2258–2268, December 2003.

[3] D. Shaeffer, T. Lee, "A 1.5-V, 1.5-GHz CMOS low-noise amplifier", IEEE Journal of Solid-State Circuits, Vol. 39, Nr. 4, pp. 569-576, April 2004.

[4] F. Alimenti, P. Mezzanotte, L. Roselli, R. Sorrentino, "Modeling and characterization of the bonding-wire interconnection", IEEE Transactions on Microwave and Techniques, Vol. 49, Nr. 1, pp. 142-150, January 2001.

[5] K. Lee, B. Park, H. Lee, M. Yoh, "Phase-frequency detectors for fast frequency acquisition in zero-dead-zone CPPLLs for mobile communication systems", Proc. of the 29th European Solid-State Circuits Conference, 16-18, Estoril, Portugal, September 2003.

[6] B. Kim, L. Kim, "A 250-MHz–2-GHz wide-range delay-locked loop", IEEE Journal of Solid-State Circuits, Vol. 40, Nr. 6, pp. 1310-1321, June 2005.

[7] S. Pellerano, S. Levantino, C. Samori, A. Lacaita, "A 13.5 mW 5-GHz frequency sinthesizer with dynamic logic frequency divider", IEEE Journal of Solid-State Circuits, Vol. 39, Nr. 2, pp. 378-383, February 2004.

[8] M. Ugajin, A. Yamagashi, J. Kodare, M. Harada, T. Tsukahara, "A 1-V CMOS SOI Bluetooth RF transceiver using LC-tuned and transistor-current-source folded circuits", IEEE Journal of Solid-State Circuits, Vol. 39, Nr. 4, pp. 745-759, May 1997.

[9] *Impexa* gigaAnt antenna datasheet, available at the gigaAnt Coorporation web site: http://www.gigaant.com.