Effects of the ESD protections in the behavior of a 2.4 GHz RF transceiver: problems and solutions

J. P. Carmo, P. M. Mendes*, F. Ribeiro*, C. Couto*, J. H. Correia*
Polytechnic Institute of Braganca, ESTiG
Campus Santa Apolonia, 5301-854 Braganca, PORTUGAL, jcarmo@ieee.org
*University of Minho, Dept. Industrial Electronics, Guimaraes, PORTUGAL

Abstract – **This paper identifies the main problems related to the Electrostatic Discharge (ESD) in submicron CMOS processes. The mitigation of this problem is made with the use of protections, in order to avoid the destruction of the internal and input/output circuits connected to the bondingpads. In the 2.4 GHz ISM band, the parallel capacitance and the serial resistance of the ESD protections have effects in the behavior of RF transceivers. The major identified effect was the transmission range. It is proposed two strategies to solve the secondary effects, due to the protections. All the measurements and simulations were made for a 2.4 GHz RF CMOS transceiver, designed and fabricated using the UMC 0.18 μm RF CMOS process.**

I. INTRODUCTION

The bondingpads are fundamental elements of an integrated circuit, e.g., they are used to connect the die to the external circuits and/or PCBs. Normally, during the chip design, it is necessary to prevent two effects that can arise: the first of them, is the latch-up. This effect can change the behavior of the circuit, as well as to destroy it [1]. Another effect, is the Electrostatic Discharge (ESD) on the die, which can cause its destruction [2]. The state-of-art shown, that ESD induced parasitics have been tolerated by regular ICs and, hence, have been largely ignored by IC designers in practices, they are becoming real limiting factors in RF and high-speed applications [3].

The scope of this paper deals with the measurement and analysis of the effects of the ESD protections in a 2.4 GHz RF CMOS transceiver. The RF transceiver under analysis, was designed and fabricated in the UMC 0.18 μm RF CMOS process. The specifications of the design, are a receiver with a sensibility of –60 dBm, with a power consumption of 6.3 mW from a 1.8 V supply. The transmitter delivers an output power of 0 dBm (1 mW) with a power consumption of 11.2 mW, for a range of ten meters. Thus, in order to comply with these specifications, the effects of the ESD protection must be taken in account (Figure 1).

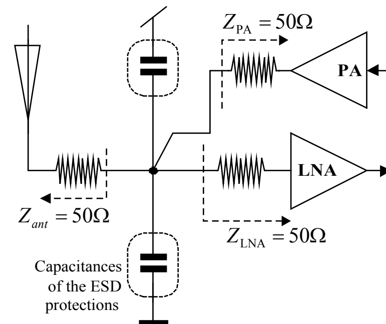


Figure 1. The effect of the ESD protections.

II. ESD PROTECTIONS

In the CMOS technology, the ESD destruction is a major concern. The destruction happens, because high currents are established, due to the breakdown of the dielectrics, where the silicon-oxides separating the gates of MOSFETs, from the channels, are an example [4]. The resulting currents can be high and melt the surface of the die, leading the circuit to the total destruction. During the design and fabrication of the RF CMOS transceiver, it was considered two levels of protections [5,6]: the first is the protection of the circuits, that connects to the bondingpads. The second level avoids the destruction of the internal circuits, from discharges coming from one of the two supply-rails (Figure 2).

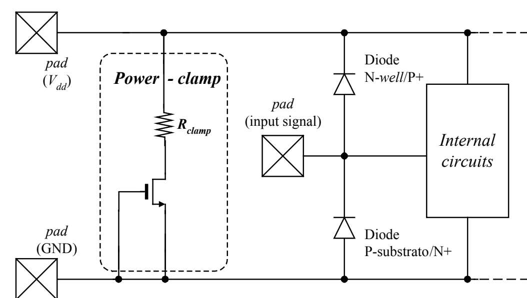
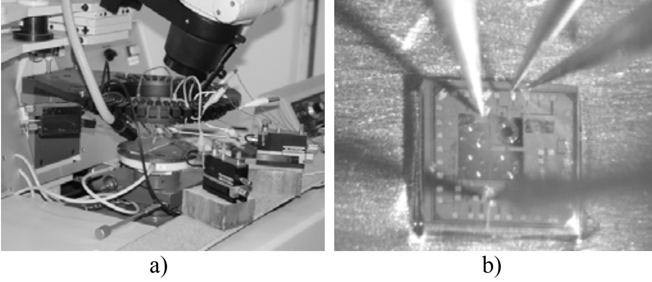


Figure 2. Protections against ESD discharges.

978-1-4244-1666-0/08/$25.00 ©2008 IEEE

III. MEASUREMENT SETUPS

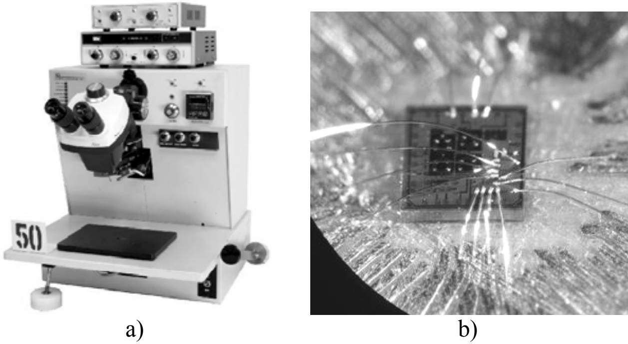
The experimental measurements were made with the help of two setups. In the first setup, it was used a probe station (model Karl Suss AP4). The Figure 3 shows the test equipment, as well as, a magnified photograph of the die and connection to the outside.



a) b)

Figure 3. a) Photograph of the probe station used in the measurements; and b) a magnified view of the die.

The second setup was made with the help of a wirebonding machine (model MEI 1204W). The Figure 4 shows a photograph of the wirebonding machine and a magnified photograph of the die. The second photograph also shows the connections between the bondingpads and the external PCB. These connections were made with Al-wires, with a diameter of 20 μm.



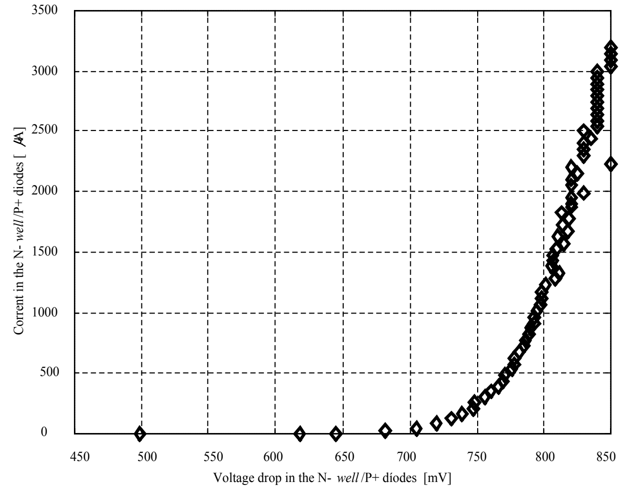
a) b)

Figure 4. a) Photograph of the wirebonding machine; and b) a magnified view of the die, during the measurements.

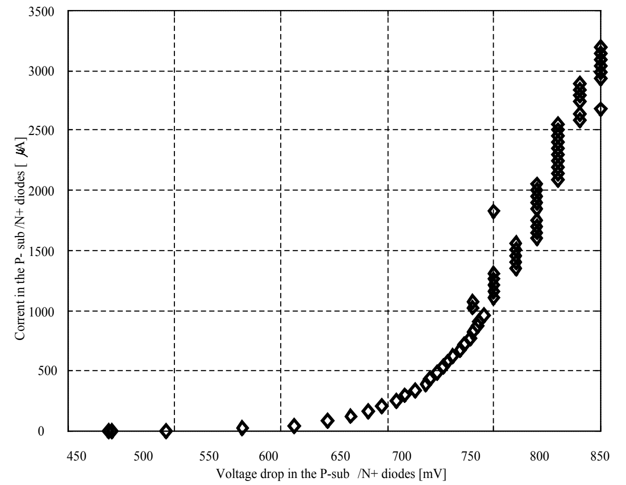
IV. EXPERIMENTAL RESULTS

The first set of tests made to the ESD protection diodes, consists in the DC voltage sweeping and in the measurement of the currents and the voltage drops in the diodes. The Figure 6 shows the I/V characteristic obtained for the P-substrate/N+ and N-well/P+ ESD protection diodes. These, were the diodes used to protect the die of discharges, cumming from one of the supply-rails (these diodes were formerly presented in the Figure 2).

It's easy to get the serial resistance (R_d) and its threshold conducting voltage (V_{th}) of the diodes, from its I/V characteristics. This is made, applying a linear fit over that characteristics. The Table 1 shows the fitting results applied to the I/V characteristics in the Figure 5.



a)



b)

Figure 5. I/V characteristics a) for the N-well/P+ diodes, and b) for the P-substrate/N+ diodes.

TABLE I. THE SERIAL RESISTANCE (R_D) AND THE THRESHOLD CONDUCTING VOLTAGE (V_{TH}) OF THE ESD PROTECTION DIODES.

	P-substrate/N+ diodes	*N*-well/P+ diodes
R_d (Ω)	25.9	25.9
V_{th} (mV)	767.2	767.2

The quantification of the capacitance associated to the ESD protections is of major interest. The value of a capacitance, for a PN junction is given by:

$$C_j = \frac{C_{j0}}{(1+\frac{V_d}{\phi_0})^m} \quad (1)$$

where, V_d is the DC reverse voltage bias, applied to the PN junction. C_{j0} is the junction capacitance with V_d=0 V, and ϕ_0 is the potential value of the junction. The capacitances of the diodes used as ESD protections, are given by:

$$C = \frac{C_j A_d}{(1+\frac{V_d}{\phi_0})^{m_j}} + \frac{C_{jsw} P_d}{(1+\frac{V_d}{\phi_0})^{m_{jsw}}} \quad (2)$$

where A_d and P_d, are the area and the perimeter of the ESD protection diodes. The used SPICE parameters are C_j=0.00119, C_{jsw}=1.6×10^{-10}, ϕ_0=0.79, m_j=0.515, m_{jsw}=0.381, for a area of A_d=675μm^2 [7]. Sweeping V_d in the voltage range [0, 1.8 V], it was obtained the worse value for the ESD capacitance. The former value is given by the sum of the capacitances, obtained for the two ESD protection diodes ($C_{nwell/P+}$ and $C_{psub/N+}$), which results equal to $C \approx 1.57$ pF. Due to this parasitical capacitor, the input of the Low-noise Amplifier (LNA) is no longer matched with the antenna. This increases the return loss at the input, making the range smaller, for the same power transmission. Calculations shown a decrease in the range, from 10 meters to 5.5 meters. Alternatively, for the same 10 meters range, the transmitted power must be 2 mW, in order to compensate the unexpected 3 dB losses.

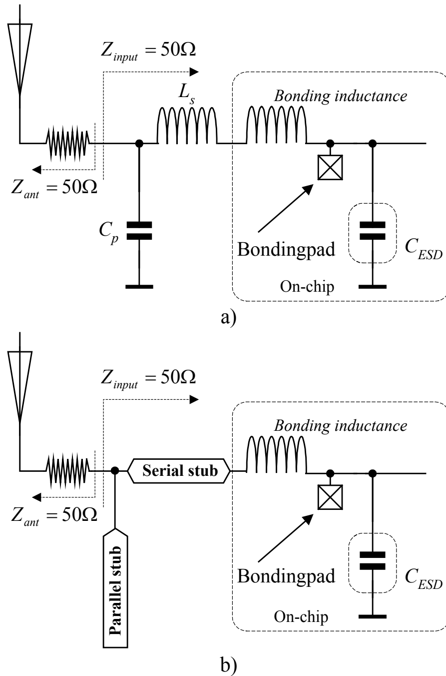


Figure 6. The simulated setups for the compensation of the ESD capacitances: a) with lumped circuit-elements, and b) with transmission lines, as circuit elements

The solution to overcome the undesired effects, is the use of external elements (lumped or distributed), in order to have again, a perfect match between the input of the LNA and the antenna. The Figure 6 shows two solutions, to improve the behavior of the circuit. The first setup is constituted by a classical matching network, which consists on a series inductance, L_s=1.5nH and a parallel capacitor, C_p=3pF. The second setup uses a series-stub (with characteristic impedance of 40 Ω and an electrical length of 30º) and a open-circuited parallel-stub (with characteristic impedance of 55 Ω and an electrical length of 69º). For the both setups, it was accounted the inductance of the bonding connection to the external PCB, which has been calculated to be 0.9 nH/mm [8].

The Figure 7, shows four situations for the reflection coefficient (k_R) at the input of the LNA: a) ideally, without the effect of the ESD protections; b) with the effect of the ESD protections; c) with a compensation (matching) network made of lumped elements, and d) with a compensation network made of transmission lines. It can be seen, that in the matching situation, the reflections decreases to acceptable values, e.g., the reflection coefficient, k_R is very close the center of the Smith's chart. Solutions relaying on transmission lines are worthable than those using lumped elements, because it is achieved a better repeatability, due to the usage of lithography processes in the fabrication. Moreover, a laser trimming technique can be used, when it is desirable a fine tuning of the transmission lines.

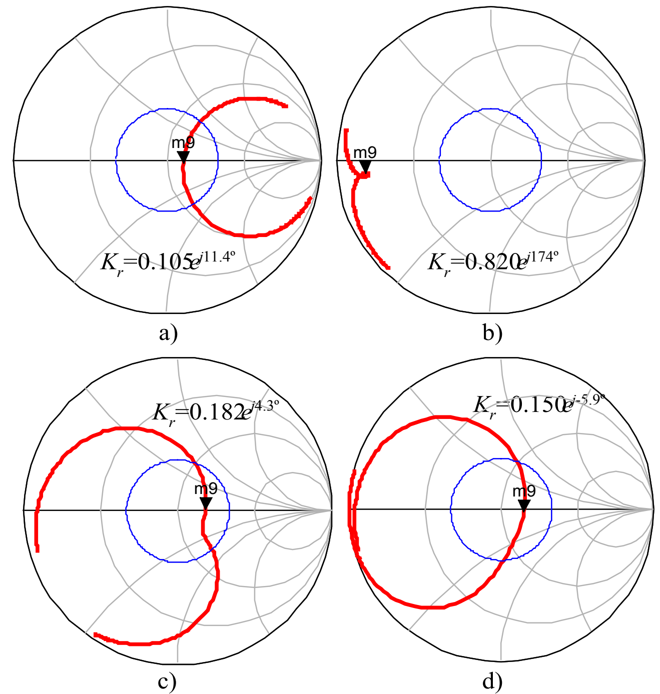


Figure 7. Reflection coefficient (k_R) a) ideally, without the effect of the ESD protections; b) with the effect of the ESD protections; c) with compensation network formed by lumped elements, and d) with a compensation network formed by transmission lines.

The Figure 8 shows the group delay in the LNA, for all the formerly cited situations. These simulations promises good potential for broad-band applications, when are used lumped elements in the matching network.

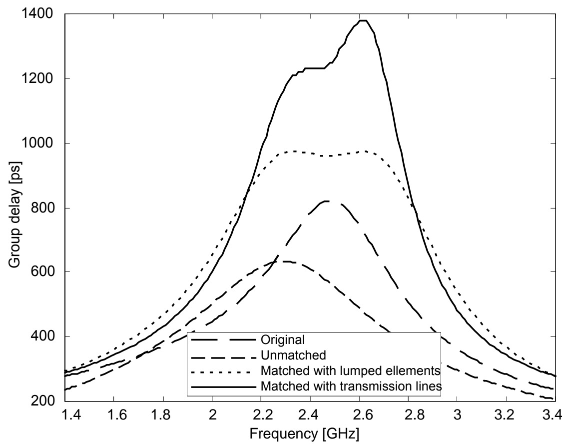


Figure 8. Group delay.

The simulations show, that forward transmission of the LNA (given by the S_{21} parameter), is improved with both matching networks. From the S_{21} point of view and excepting the fabrication issues, any matching technique can be selected without special concerns (Figure 9).

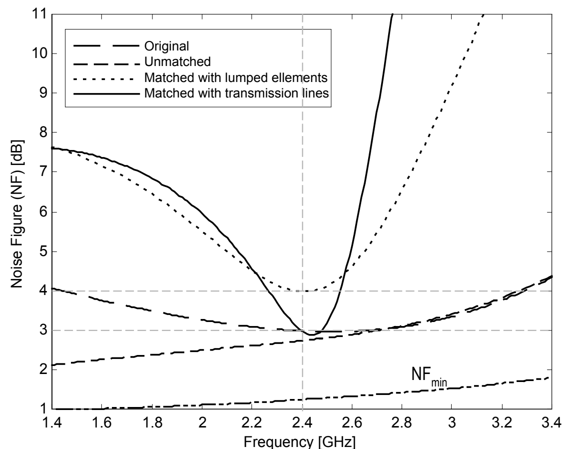


Figure 9. NF [dB] of the LNA.

Finally, the Figure 10 shows the behavior of the noise figure (NF). It can be seen that the worse (but still acceptable) situation occurs with the use of lumped elements in the matching network. On this situation, the NF is located around the 4 dB. The remained situations show a NF below (but very close) the 3 dB.

V. Results discussion and conclusions

If ESD protections are used in the radio-frequency (RF) paths, specially in the inputs of the LNAs, its parasitical capacitance can affect the behavior of the entire receiver.

This paper identified the main problems concerning the ESD protections of a fabricated RF CMOS transceiver for the operation in 2.4 GHz ISM band, and presented two techniques to overcome them. The first technique uses lumped elements as matching networks, and the other uses transmission lines. The last technique has an advantage over the first, because it uses lithography in the fabrication, thus, it is favored the repeatability of the matching networks.

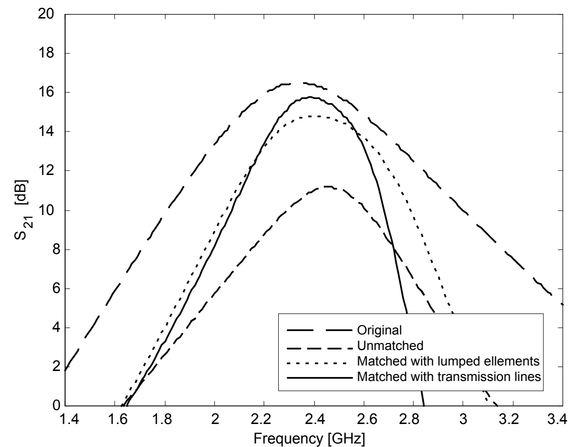


Figure 10. S_{21} [dB] of the LNA.

Finally, a special note concerned with the impact of the ESD capacitance in the transmitter, must be made. The future work deals with the characterization of the impacts in the transmitter, specially, the design of the power amplifier.

Acknowledgment

This work was sponsored by FCT/REEQ/379/EEI/2005.

References

[1] M. Ker, W. Lo, “Methodology on extraction compact layout rules for latch-up prevention in deep-submicron bulk CMOS technology”, IEEE Transactions on Semiconductor Manufacturing, Vol. 16, Nr. 12, pp. 319-334, May 2003.

[2] J. E. Vinson, J. J. Liou, “Electrostatic discharge in semiconductor devices: An overview”, Proceedings of the IEEE, Vol. 86, Nr. 2, pp. 399-418, February 1998.

[3] H. G. Feng, *et al.*, "Electrostatic discharge protection for RF integrated circuits: new ESD design challenges", Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, Vol. 29, pp. 5-19, 2004.

[4] M. Ker, *et al.*, "Design and analysis of on-chip ESD protection circuit with very low input capacitance for high-precision analog applications", Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, Vol. 32, pp. 257-278, 2002.

[5] M. Ker, *et al.*, “Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI”, IEEE Transactions on Electron Devices, Vol. 46, Nr. 1, pp. 173-183, January 1999.

[6] M. Ker, *et al.*, “ESD implantations for on-chip ESD protection with layout consideration in 0.18-µm salicided CMOS technology”, IEEE Transactions on Semiconductor Manufacturing, Vol. 18, Nr. 2, pp. 328-337, May 2005.

[7] UMC 0.18µm 1P6M salicide mixed-mode/RF CMOS model, Giga Soluction Tech. Co. Ltd., UMC Doc. No. 04U1-02034, Ver. 2d2, March 2002.

[8] F. Alimenti, *et al.*, "Modeling and characterization of the bonding-wire interconnection", IEEE Transactions on Microwave and Techniques, Vol. 49, No. 1, pp. 142-150, January 2001.