PLL at 2.4 GHz with reduced reference spurs

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***Abstract*—This paper presents a frequency synthesizer for the frequency of 2.4 GHz, which were designed to present a reduced level of reference frequency spurs. Parts of the synthesizer were fabricated in a standard 0.18 µm CMOS process, whose architecture is based on a Phase-Locked Loop (PLL) with an integer divider in the feedback loop and was designed to work with a voltage supply of only 1.8 V. Some building blocks are reused thus the novelty of this paper is presenting a PLL with two new blocks for reducing the magnitude of spurs of the .process, e.g., a sample-and-hold circuit and a quantizer circuit (with *N* quantizing levels). The PLL behaviour was simulated for a few number of levels - *N*={32, 64, 128} - and for a variety of loop-filters. As showed by the simulations, the quantizations provide an additional reduction of the reference-frequency spurs into the output of the PLL. Moreover, the locking time is kept low even after including the two new circuit blocks in the loop**

Keywords: PLL, CMOS, wireless microsystems.

I. INTRODUCTION

THIS paper presents a low-voltage frequency synthesizer for operation in the 2.4 GHz ISM band for use in Wireless Personal Area Networks (WPANs). The synthesizer is a Phase-Locked Loop (PLL) with an integer divider in the feedback loop, which was designed and fabricated in a standard 0.18 µm CMOS process for achieving a high degree of integration and at the same time allowing the use of the low-voltage of only 1.8 V to supply the chip.

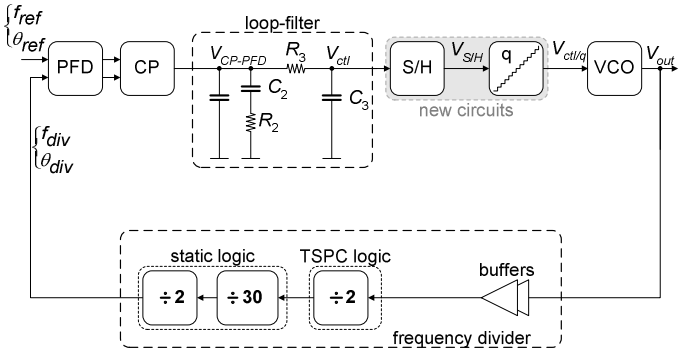

Figure 1. The structure of the PLL after including two new circuits (the sample-and-hold and the quantizing circuits) into the loop.

The PLL presented in this paper reuses circuit blocks that were already subjected to previous validation (e.g., the Voltage-Controlled Oscillator, VCO; the Phase/Frequency Difference, PFD, circuit; the Charge-Pump, CP, circuit; the loop filter, LF; the frequency divider with a dividing ratio of M=120; and the crystal oscillator circuit for generating the reference frequency) and two new blocks (e.g., a sample and hold circuit, S/H, and a quantizer circuit) [1]. The PLL behaviour was analyzed for a set of four loop-filters (that were obtained for the respective set of targeted specifications) and for the given number of quantizing levels: N=32, N=64 and N=128. The quantity N=16 was simulated only for one filter.

II. THE FREQUENCY SYNTHESIZER ARCHITECTURE

A. Architecture

The 2.4 GHz frequency carrier is generated by means of a local oscillator, which is a Phase-Locked Loop (PLL). As showed in Figure 1, the PLL has a reference generator circuit with a crystal based oscillator at 20 MHz (the value of f_{ref} [Hz]), followed by a phase-frequency difference circuit (PFD) without dead zone, a current steering charge pump (CP) and a third order passive filter (LF). The sample-and-hold is putted before the quantizer circuit and both are connected between the VCO and the loop-filter. Then, the output of the VCO (whose signal is desired to be at the 2.4 GHz frequency) closes the loop by connecting to the divider circuit with the help of a buffer. This frequency must be divided by 120 (the division ratio, M=2×30×2, at the feedback path, which is digitally selectable) and connected to the PFD again, closing the loop. From the available categories found in the literature (e.g., integer or fractional divider ratios in the feedback path [2]), this PLL uses the technique of integer dividing in the feedback path with $f_{out} = M.f_{ref}$.

The selection of the frequency dividing technique was done taking in account that in fractional PLLs, a lot of cares are required for avoiding multiple values of the reference frequency in the output [3,4], because f_{out} changes in multiples of the reference frequency, due to the removing of one pulse in the feeding-back signal (just before the re-injected in the PFD) at each T_p[s]. This allows the operation of fractionally dividing the output frequency, obtaining $f_{out}=M.(f_{ref}+1/T_p)$. Thus, in spite of the fractional PLLs allowing a finer adjust of f_{out}, the former drawback was the main criterion towards the selection of an integer PLL.

B. Ripple reduction

It is well know that the first-order section of the loop-filter (that is constituted by R_3 and C_3) is used to reduce the ripple of the signal V_{CP-PFD} [V]. However and even with such a filter, a significant level of ripple is expected to be present in the

filtered signal, V_{ctl} [V]. The technique presented in this paper samples the signal at the output of the loop-filter and quantizes such a sample. By sampling V_{ctl} during finite time intervals, it is expected a reduced impact of their fluctuations in the signal at the output of the PLL. Figure 2 illustrates this concept with an expectation of a smaller ripple for smaller values of N. However and as it will be further observed, it is expected also an increase in the time required for the PLL to lock. This means that selection of the quantizing levels, N, is subject to a trade-off between the ripple and the time to lock.

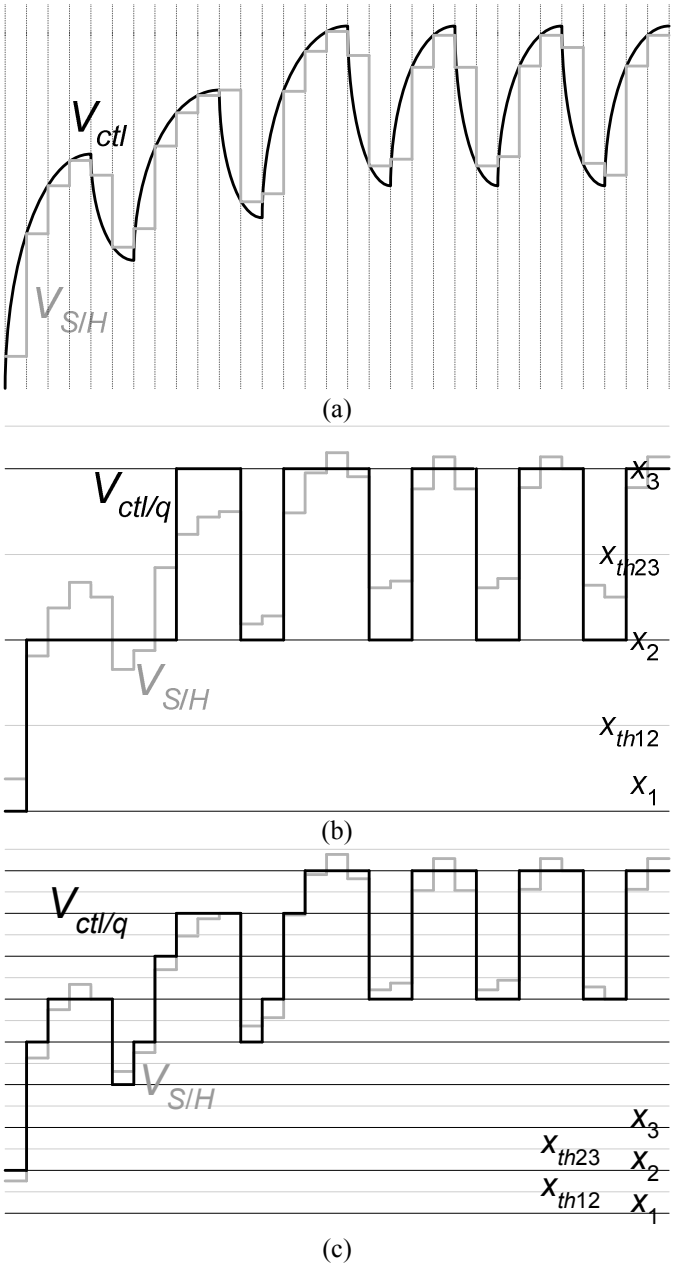

Figure 2. The illustration of the proposed concept: (a) after sample and holding the signal at the output of the loop-filter, obtaining $V_{S/H}$ [V]. The quantized versions of the signal $V_{S/H}$ are depicted for (b) a given number, N, of quantizing levels (10 transitions), and (c) with an increased number of levels (16 transitions). More quantizing levels implies more transitions, increasing the ripple and making the reference spurs to increase in the output of VCO.

In Figure 2 it is possible to observe that an increase in the quantizing levels, N, will result in more transitions, but with a small degree of abruptness.

III. VALIDATION

A. Loop-filter analysis

The stability of a PLL is ensured with a phase margin at least of $\pi/4$ rad [5]. The definition of this value as well as the definition of the two following parameters is the starting point for obtaining the filter components [5]: (1) the bandwidth, f_p [Hz], the phase margin ϕ_p [rad], (2) the minimum attenuation, A_{min} [dB], measured at multiples of the spurious reference frequency, f_{ref} [Hz], which is imposed by the low-pass filter R_3C_3. This allows the determination of the three time constants, T_1, T_3 and T_2:

$$T_1 = \frac{\frac{1}{\cos(\phi_m)} - \tan(\phi_m)}{2\pi f_p},\ T_3 = \frac{\sqrt{10^{\frac{A_{\min}}{10}} - 1}}{2\pi f_{ref}} (= R_3 C_3),\ \text{αvδ}\ T_2 = \frac{(2\pi f_c)^{-2}}{T_1 + T_3} \quad (1)$$

The first loop-filter components are then given by the following equation:

$$C_1 = \frac{T_1 K_\phi K_{VCO}}{T_2 (2\pi f_p)^2 N} \times \sqrt{\frac{1 + (2\pi f_p)^2 T_2^2}{[1 + (2\pi f_p)^2 T_1^2] \times [1 + (2\pi f_p)^2 T_3^2]}}$$
$$C_2 = C_1 \left(\frac{T_2}{T_1} - 1\right), \text{ and } R_2 = \frac{T_2}{C_2} \quad (2)$$

Finally, the remaining loop-filter components R_3 and C_3 are obtained as follows [5]:

$$C_2 = C_1 \left(\frac{T_2}{T_1} - 1\right) \quad \text{, and} \quad R_3 = \frac{T_3}{C_3} \quad (3)$$

The passive components of the loop-filter were selected after applying few specifications in the previous equations. Table I show the loop-filter components and the most significant results (darker gray cells) for the targeted specifications (the gray cells on the superior part of the table). It must be noted that the used VCO allows for tuning the full range [0, 1.8 V] and that the simulations considered the tuning constant K_{VCO}=876.6 MHz.V^{-1} obtained from the linear working range. The simulations also took in account a charge-pump with a detector constant gain K_ϕ=175 μA/2π rad.

The previous work used the filters of Table I [1], but without the sample-and-hold and the quantizer circuits. It was showed that the PLL was very fast to lock. However, the undulation in the control voltage of the VCO is still insidious, making the PLL to still present spurs of the reference frequency. The goal of these two additional circuits is to keep

the time to lock acceptably low and at the same time to reduce the undulations of the VCO control voltage.

TABLE I. SPECIFICATIONS (THE CELLS ON THE SUPERIOR PART OF THE TABLE WITH GRAY-SHADING), PASSIVE COMPONENTS OF THE LOOP-FILTER AND THE MOST SIGNIFICANT RESULTS (THE CELLS WITH DARKER GRAY) [1].

Parameters	Filter #1	Filter #2	Filter #3	Filter #4
Phase margin - ϕ_m [°]	45	55	45	45
Bandwidth – f_p [MHz]	1.2	1.2	1.2	0.8
Frequency f_c [MHz]	0.82	0.75	0.64	0.51
Attenuation A_{min} [dB]	10	10	15	15
C_1 [pF]	10	11.7	18	35
C_2 [pF]	81	180	185	300
R_2 [$k\Omega$]	5	3.7	3.5	2.7
C_3 [pF]	1	1	1.5	3.5
R_3 [$k\Omega$]	20	20	17.5	11
Actual phase margin [°]	44.8	55.3	49.1	45.6
Dumping - ξ	0.76	0.86	0.81	0.79

B. *Results*

The four filters whose passive components are listed in Table I were used to validate the proposed concept. In the previous work, the first filter (#1) was the one that made the PLL to lock with the smaller time. As further presented, including the two new circuits in the direct branch keeps this tendency independently of the number of quantizing levels, N, (for a reasonable number of levels, e.g. $N \in \{32, 64, 128\}$).

The simulations results in Figure 3 were obtained for the first filter of Table I and are parameterized for the following quantizing levels: $N \in \{16, 32, 64, 128\}$. The case of N=16 was quickly discarded due to the degradation that were observed in the locking time and at the same time due to the high-amplitude oscillations around the permanent regime value (i.e., for $V_{ctl/q}$ [V]). It is interesting to observe that after 3 µs, the mean value of $V_{ctl/q}$ is about 0.87 V.

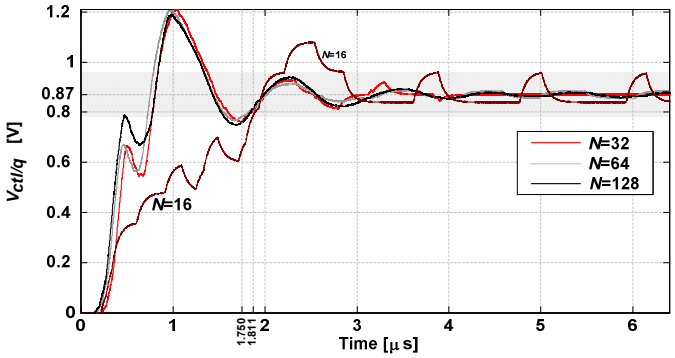

Figure 3. Behaviour of tuning voltage of the VCO, $V_{ctl/q}$ [V], for the first filter of the Table I and for several number of quantizing levels, N.

The time to lock resulted in simulations of Figure 3 is almost the same for any N except 16 (a large time to lock and residual oscillations with high amplitude). For this filter, the time to lock is in the range [1.750, 1.811] V. The shading area in gray defines the border when the PLL is considered to be locked. The limits of this area are 10% above and below the final value, $V_{CTL/q} \approx 0.87$ V. The instants where the lines cross these borders for the last time are considered the times that the PLL take to lock.

The behavior of the voltage at the output of the charge-pump, $V_{CP\text{-}PFD}$ [V], and the voltage at the output of the loop-filter (just before the sample-and-hold circuit), V_{ctl} [V], are illustrated in Figure 4. It is possible to observe that for three simulated cases ($N \in \{32, 64, 128\}$, the case of N=16 was excluded due to its shortcoming to achieve the targeted goal – e.g., small ripple in the VCO control voltage) both the signals present ripple susceptible to increase the sensitivity of the VCO to spurs of the reference voltage.

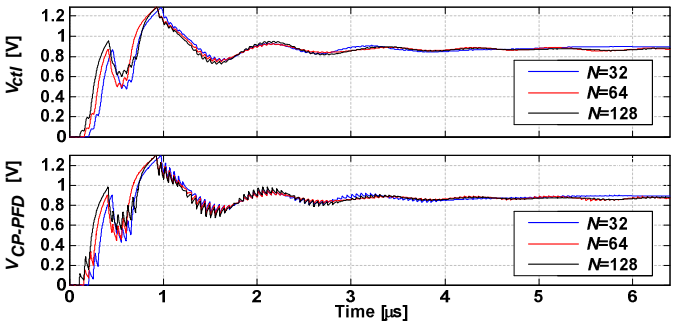

Figure 4. For the first filter in Table I and $N \in \{32, 64, 128\}$: (top plot) the voltage at the output of the loop-filter, which is the voltage in the node just before the sample-and-hold circuit, V_{ctl} [V]; and (bottom plot) the voltage at the output of the charge-pump, $V_{CP\text{-}PFD}$ [V].

A simple analysis of Figure 4 and the existence of ripple without practical interest allow concluding on the worthless to repeat these plots again for the three remaining filters of Table I. In this sequence of ideas, the focus is kept on the $V_{CTL/q}$ voltage.

The simulation results showed in Figure 5 are the behaviour of the voltages $V_{ctl/q}$ [V] that were obtained for these number of quantizing levels $N \in \{32, 64, 128\}$ and for each of the filters #2, #3 and #4 in the Table I.

As it was expected and comparing with the previous results in [1], the time to lock is higher for the filter #2 than for the filter #3, as well as the filter #3 to the filter #4. It is interesting to note that with these three filters, the smaller time is achieved with N=32 (the blue lines on both three plots). It can be observed that the time to lock for PLLs with the first three filters (defined for a bandwidth of 1.2 MHz) is in the range [1.75, 2.25] µs, whereas this time is higher and in the range [2.75, 3.25] µs for PLLs with the fourth filter (defined for a bandwidth of 800 KHz).

Of course it is passive the acceptance the fact that the bandwidth explains the fast or slow convergence of the PLL, but what is not explained is the possible cause to the

high-spanning in the time to lock for N=32 and the remaining Ns for the filters #3 and #4. A possible explanation resides in the minimum attenuation, A_{min} [dB], measured at multiples of the spurious reference frequency that was targeted for obtaining the loop-filters. In this sequence of ideas, it is possible to observe in Table I that contrary to the first two loop-filters (that were obtained for A_{min}=10 dB), the last two were obtained for an attenuation A_{min}=15 dB.

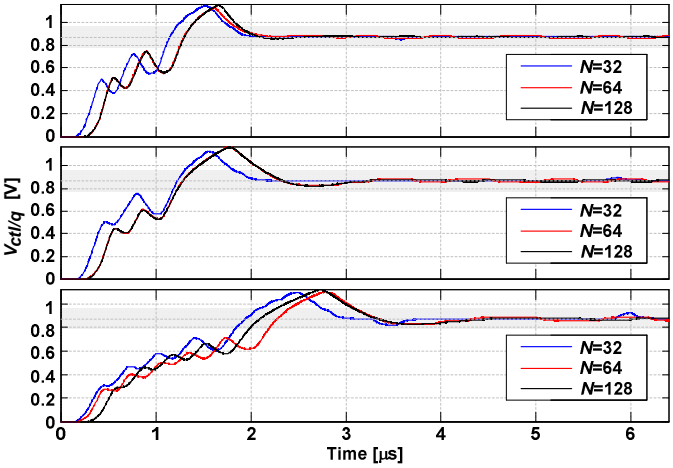

Figure 5. Behaviour of tuning voltage of the VCO, $V_{ctl/q}$ [V], for several number of quantizing levels, N, and for the remaining three filters of the Table I: (top plot) filter #2, (mid plot) filter #3 and (bottom plot) filter #4.

An interesting (but also expected) conclusion is the fact that the permanent regime value of the quantized voltage at the input of the VCO is allows the same, e.g., $V_{CTL/q}$≈0.87 V.

The observations of Figures 3 and 5 also result in an intuitive and expectable conclusion: the oscillations of $V_{CTL/q}$ around the final value of 0.87 V decreases when N increases.

For applications were the locking time is a critical factor, a filter with high bandwidth and an acceptable phase margin (at least a targeted value of ϕ_m=45º) and attenuation A_{min} (for example, A_{min}=10 dB) must be provided with a moderate number of quantizing levels (at least N=32).

It was notorious the absence of ripple on all voltages $V_{CTL/q}$ that were obtained with the expected consequence to have small spurs of the reference frequency, f_{ref} [Hz], and low-drift caused by the temperature. Moreover, as it happened with N=16, the mean value of $V_{CTL/q}$ for the other Ns is approximately 0.87 V after the PLL entering in the lock status.

Figures 6 and 7 show the normalized spectrograms of the VCO outputs for N=128 and N=64. These spectrograms display the temporal evolution of the signal spectrum and as it can be observed, their lateral spreading are low and follows the (theoretical) central instantaneous frequency, f_{out} [Hz].

Another test was done by replacing the fixed frequency divider by M=120 with a selectable frequency divider. The new frequency divider was chosen for allowing the selection between M=120 and M=124, e.g. for generating either 2.4 GHz or 2.48 GHz. Figure 8 also shows the temporal evolution of signal spectrums of f_{out} [Hz] for N=32, N=64 and N=128. The evolution of the control voltage, $V_{ctl/q}$ [V], can be observed in the 1st quadrant where are displayed the selected division ratios M (either M=120 or M=124). The filter #1 was the only one to be considered because it is the one that results in the fastest locking times. From the simulations in Figure 8 it is possible to observed the good behaviour of the altered PLL (e.g., with S/H and quantization circuits) when the frequency is switched. This is of major importance to apply the proposed concept into DSSS systems.

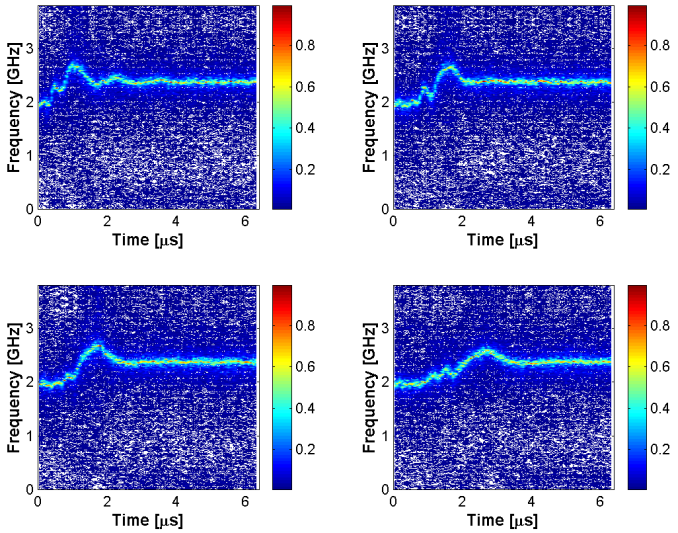

Figure 6. For N=128 quantization levels: temporal evolution of signal spectrums (oscillograms) at the VCO output for each one of the four loop-filters. The plots for the filters #1, #2, #3 and #4 are depicted in the figures located at the 3rd, 2nd, 4th and 1st quadrants, respectivelly.

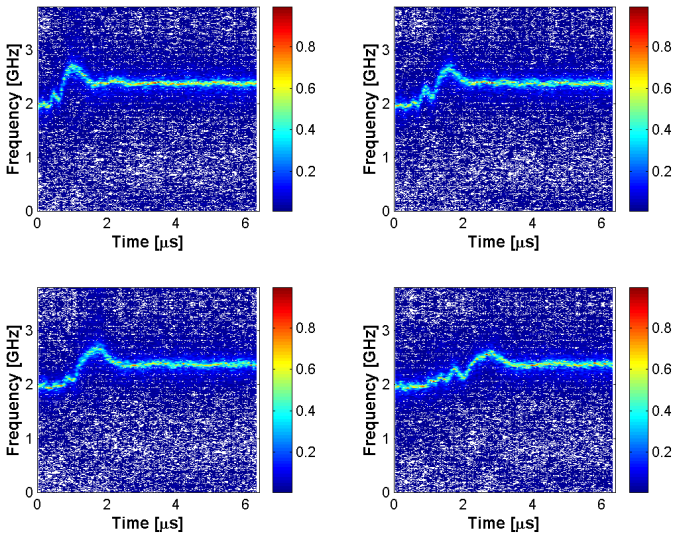

Figure 7. For N=128 quantization levels: temporal evolution of signal spectrums (oscillograms) at the VCO output for each one of the four loop-filters. The plots for the filters #1, #2, #3 and #4 are depicted in the figures located at the 3rd, 2nd, 4th and 1st quadrants, respectivelly.

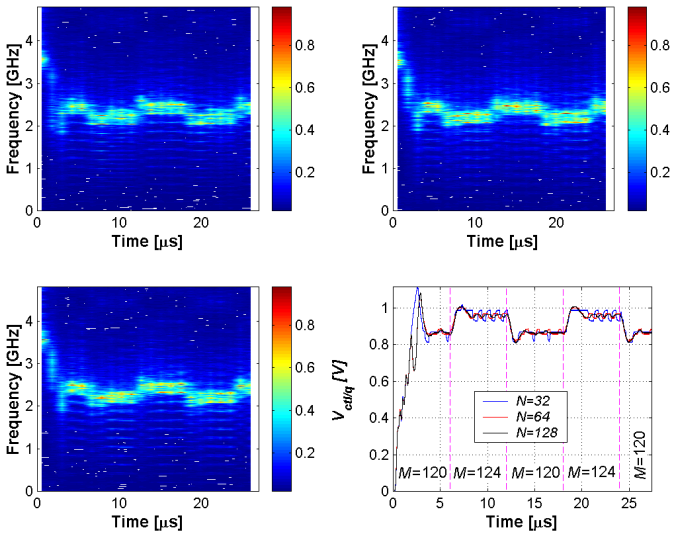

Figure 8. Temporal evolution of signal spectrums (oscillograms) at the VCO output for N=32 (3rd quadrant), N=64 (2nd quadrant) and N=128 (4th quadrant). The three signals of plot at the 1st quadrant shows the voltage control, $V_{ctl/q}$ [V], for division ratios of M=120 (f_{out}=2.4 GHz) and M=124 (f_{out}=2.48 GHz) and where obtained with the filter #1.

IV. CONCLUSIONS

This paper presented a PLL at 2.4 GHz, which were designed to reduce the magnitude of the spurs of the reference frequency, f_{ref} [Hz] as well as a reduced frequency drift. The behaviour was simultaneously simulated for N={32, 64, 128} and for a different number of loop-filters. Globally, good results were obtained for a few situations, e.g., low degree of ripple in the voltage at the input of the VCO. The quality of results is in the same order of magnitude of the previous work [1] but with the added advantages of the proposed concept.

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