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INTELLIGENT SIGNAL PROCESSING FOR RATIOMETRIC DATA ACQUISITION: A LOW COST SOLUTION FOR LOAD CELLS

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ABSTRACT

This paper describes a data acquisition solution using a single chip risc type microcontroller with very few other active and passive components around. The need for thermally stable circuits and components is minimized through the use of the same amplification chain for both the signal and reference, together with software calibration. The analog to digital conversion is done using the single ramp approach controlled by the microcontroller which does all the digital processing required as well as the serial communication with the external world. The paper also describes an example of software calibration of a multi-loadcell weighbridge using one single processing module per sensor.

Keywords: *Data Acquisition, Intelligent Transducers.*

INTRODUCTION

Multi-load-cell weighing systems normally use a single signal processing circuit with the individual load cells outputs tied together. Because tuning the gain of a load cell affects the behavior of the others, calibration is difficult and tedious, specially with weighbridges for car and trucks, requiring the motion of heavy weights around large platforms.

The use of load cells with digital outputs, i.e., with integrated signal processing, allows the gain adjustment to be a simple multiplication of the load cell output by a coefficient, operation which does not affect the other load cells outputs. In this case, the calibration process means the calculation of the multiplying coefficients, which are given by the solution of a set of equations, operation easily performed by any general purpose microcomputer.

However this solution although greatly reducing the commissioning time of weighbridge, type equipment needs a cost effective solution for the load cells data processing so that is not uneconomical to use one per transducer.

Having in mind industrial weighing applications where 6000 divisions are needed for the equipment (external divisions) a conversion resolution of at least 60000 divisions (10 internal divisions for each external) with 20 or more readings per second, at least for static weighing applications. For dynamic weighing a faster reading rate is required but with lower resolution

For the specifications referred there are already suitable components in the market, namely amplifiers and A-D converters [1,2], some of these even with networking facilities [2]. However some other facilities toward intelligent sensing [3] are also desirable: amplifier gain and OFFSET adjustment controlled by software, scaling and eventually digital filtering of the converter results. These requirements needs extra hardware namely a processing capabilities. Once the microprocessor is needed, the all architecture should be rethought in order to maximize its use reducing the hardware and its specifications.

This contribution describes a feasibility study towards a solution for the problem taking advantage of the high performance low cost microcontrollers available today and of the ratiometric functioning of the load cells [6].

SIGNAL PROCESSING CIRCUIT

Design Strategy

Fig 1 shows the conceptual ideas behind the proposed circuit.

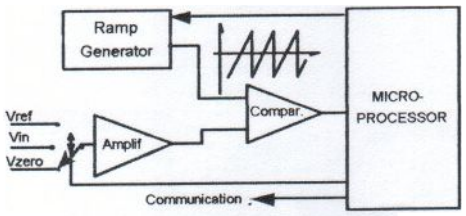

Fig.1 - Circuit block diagram

The same amplifier chain is properly switched to deal with the zero, the load cell signal and the conversion reference. In this way the thermal stability requirements for the amplifier can be relaxed as a change in gain will affect all the three entities defining the A-D conversion. A simpler architecture can be used just enough to ensure that the gain remains constant during the conversion period.

A single ramp conversion was used because it requires the minimum hardware and with the same grade components, it allows a higher rate of conversions. However this simple conversion technique is not intrinsically compensated as dual ramp conversion for example, requiring some pos-conversion processing specially in this case where the zero, the signal and the reference are allowed to change.

The counting associated with the single ramp A-D conversion, the control of the switches in the amplifier stage and the control of the ramping capacitor discharge are tasks to be performed by a microprocessor architecture. Some number crunching to work out the conversion result which may include scaling and eventually some digital filtering and the communication with the outside world, are the other tasks to the microprocessor.

Fig.2 shows the conversion process and the related calculations required.

To minimize the hardware and to reduce the errors the same comparator is used to detect the three level crossings. Normally these comparisons are done one on each ramp, therefore requiring three ramps [1]. In this case the three comparisons are done during the same ramp reducing the conversion time to a third. All it is needed is to allow enough time to switch the amplifier chain from one signal to the other until there is stable output. This was accomplished in the conversion by restricting (Vinmin-Vzero) and (Vref-Vinmax) to be _ _V volts to allows the transients to settle. With this strategy the Vin range is reduced but the precision of the conversion is improved as the denominator is increased, as can be seen in the expression giving the conversion result.

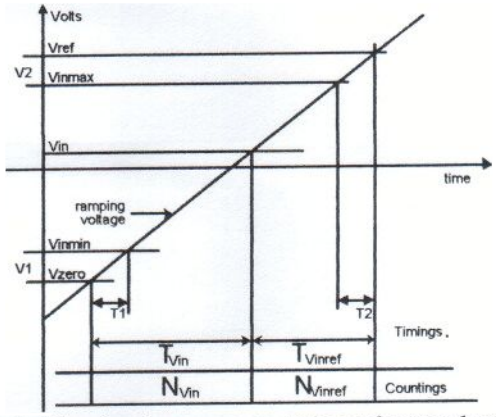

Fig.2- The single ramp conversion scheme adopted

The conversion result is given by the expression below, where N_{Vin} represents the time for ramp to reach the signal voltage, while N_{Vinref} represents the ramp time between Vin and Vref. N_k is a normalizing factor.

$$Conversion = \frac{N_{Vin}}{N_{Vin} + N_{Vinref}} \times N_k$$

Circuit Implementation

Fig.3 shows the circuit implemented for this feasibility study comprising the digital processor /controller, the amplifier and the conversion.

The Controller: The circuit was developed around an 8 bit single chip Harvard architecture microcontroller with RISC-like features, the PIC16C54, recently introduced in the market by MICROCHIP, with interesting characteristics for this type of application:

-low cost.

-only 33 single word instructions .

-operating speed: DC - 20MHz clock input (200ns instruction cycle).

-all single cycle instructions (200ns) except for program branches which are two-cycles.

-small size with EPROM.

-8 bit real time timer/counter.

-Low power consumption (< 2mA a 5V).

Although there are no interrupt facilities, neither pin driven nor triggered by timer/counter overflow, because its reduced instruction cycle time and its very low cost, it was decided to use this microcontroller requiring a more software intensive solution.

At a later stage it is planned to use the PIC17C42, a faster chip with the same architecture but with a higher performance and more peripherals: clock frequency up to 25MHz, serial port communication with baud rate generator, three 16 bits timer/counters, two PWM outputs and 11 external/internal interrupts.

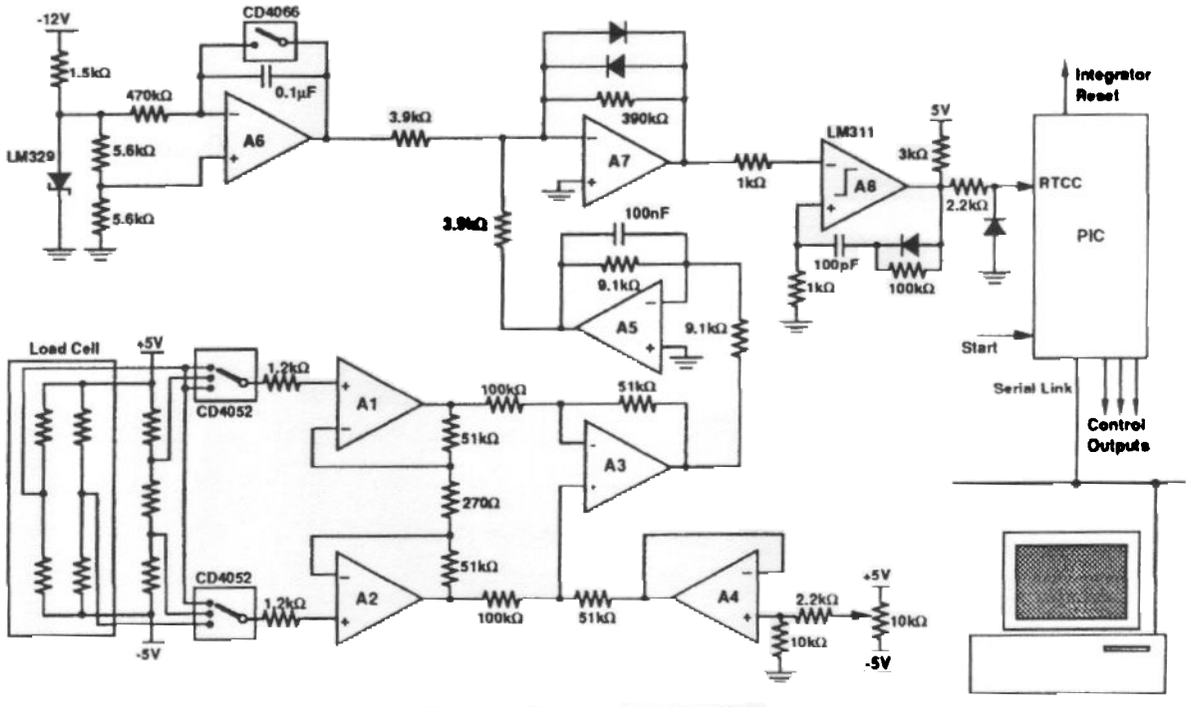

Fig.3- The signal processing circuit diagram

The Amplifier Stage: A standard instrumentation amplifier (A1, A2 and A3) was build with a fixed gain configuration. The offset is adjusted with a potentiometer coupled to the circuit through a buffer amplifier (A4).

The inputs of the instrumentation amplifier is switched between zero, the load cell and the reference voltage through a dual 4-to-1 multiplexer (CD4052) driven by the microcontroller. The zero signal is obtained short-circuiting the two inputs, while the reference is given by a voltage divider across the load cell feeding voltage.

A1, A2, A3, A4 are implemented through the quad BIFET OP AMP TL084, a bipolar operational amplifier with FET inputs to reduce the input bias currents [5]. The reference voltage divider resistors were chosen with very low temperature coefficient, while the others are the common metal film resistors with ±50ppm/°C.

The Ramp Generator: The integrator circuit build with A6 implements this function. The switch CD4066 driven by the PIC16C54 discharges the capacitor to restart the ramp. To have a stable slope the reference zener voltage LM329 was used to define the integrating current. Also a polypropylene integrator capacitor, with low dielectric absorption, was used to guarantee the constant slope independent of the A6 output voltage.

The Comparator: To assure a faster and more sensitive comparison at A8 the OPAMPs A5 and A7 were used: A5 inverts and does some filtering to the A3 output, so that at the A7 input summing point, the current due to the ramp is subtracted from the current proportional to the signal. When this current difference is large A7 operates at a low gain due to the diodes in the feedback loop. When the currents produced by the ramp potential and A5 very nearly balance, the potential at A7's summing junction will go low enough, so that A7 comes out of the diode bounding and operates with a gain determined by the feedback resistor (390k_) [1]. The A7 makes the A8 comparator's job much easier, it amplifies the voltage difference of the two signals to be compared by a factor of 100, reducing the A8 input uncertainties. The components in the positive feedback path at A8 ensure a sharp transition.

The Conversion Algorithm: When a start conversion command is received the microcontroller switches the comparator input to the zero position and waits until the ramp crosses -3V. Then it switches the amplifier input to the Vin position (load cell outputs) and measures (counts) the amount of time (N_{Vin}) required for the ramp to cross Vin. As soon as this occurs it switches to the full scale reference voltage and measures the time (N_{Vinref}) required for the ramp to cross Vref. With all this information and the assuming that Vref and Vin don't vary during the conversion time, the 5 digit numerical value of Vin is determined by the following equation:

$Vin=[N_{Vin}/(N_{Vin}+N_{Vinref})]*K$, with K=100000.

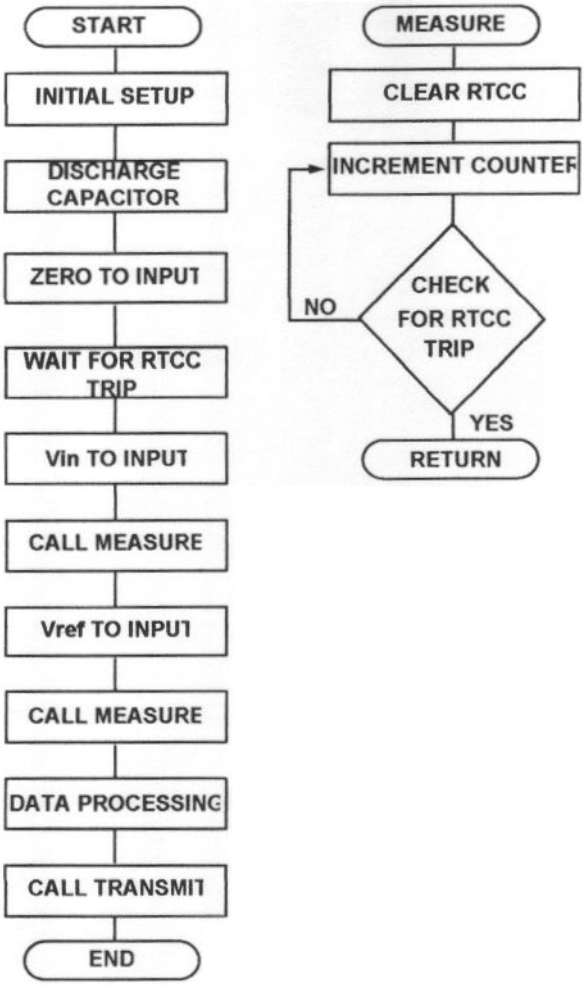

Fig.4 - Conversion Flowchart

Fig.4 shows the flowchart concerning the conversion software. Because the counters were implemented by software, measure subroutine in the flowchart was in fact replaced by its code.

The implementation of the 16 bit counters required a special care to achieve the high speed without loosing countings, even when two bytes needs to be incremented.

Experimental Results

The instrumentation amplifier has a gain of 194 and its offset was adjusted to give -3V with the inputs are short-circuited. The microcontroller driven by a clock frequency of 16MHz (250ns instruction cycle) gives a counting period of 1.5µs. The integration components, R=470k_ and C=0.1µF gives the described by the equation,

$$V_{O6}(t)=-3.445+73.29t \quad (t \text{ in secs})$$

and shown in fig.5. The voltage divider was designed to produce at A3 output a reference voltage around 3.2V. The Vin's range was defined to be between -2.5V and +2.5V.

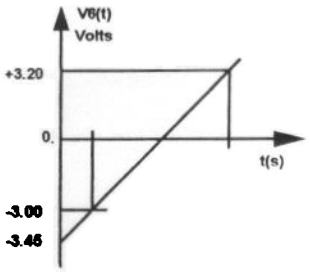

Fig.5 - A6's output ramp.

In fig.6 a screen plot of a Tektronix 2230 digital oscilloscope presents the A6 ramp output and the A7 output, before and after the crossing occurs, with the three pulses.

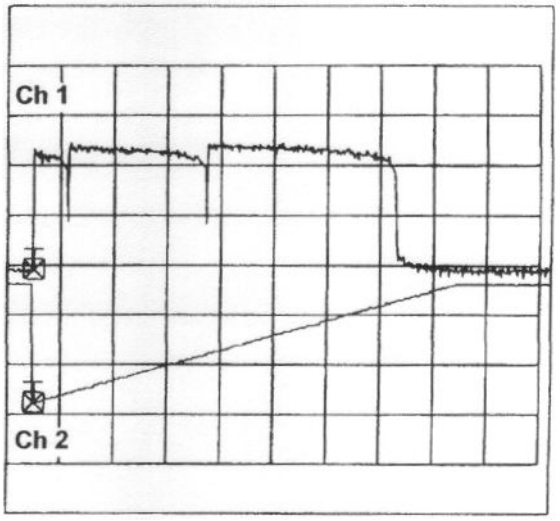

Fig.6 - Screen plot of A6 and A7 outputs. (Ch1 1V/div = A7 output, Ch2 – 5V/div = A6 output, Time base 20ms/div)

Fig.7 shows an example for a given Vin and Vref=5.1V, waveform Ch-1 is the instrumentation amplifier output, illustrating the input signal switchings, and the Ch-2 waveform is the ramp.

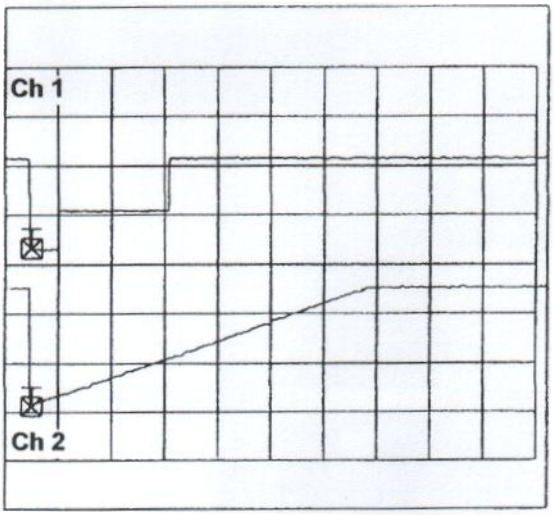

Fig.7 – Screen plot of A3 and A6 outputs (Ch1 = 5V/div = A3 output, Ch2 = 5V/div = A6 output, Time base 20ms/div).

The table below shows the sets of conversion results for different inputs.

Input Values	Vin1	Vin2	Vin3	Vin4
Conversion Results	74343	91238	81306	48953
	74346	91237	81311	48954
	74347	91239	81309	48958
	74349	91241	81318	48956
	74341	91231	81314	48946
	74346	91229	81318	48955
	74347	91238	81316	48945
	74348	91232	81316	48958
	74343	91244	81310	48958
	74346	91238	81319	48953
Average	74346	91237	81314	48954
Deviation	-5 , +3	-6 , +7	-8 , +5	-8 , +4

The conversion time obtained was around 95msecs, time which can be reduced by increasing the microcontroller clock frequency up to 20 Mhz. Using PIC17C42 at 25 MHz further improvements can be obtained with hardware counting. The resolution attained of 63000 divisions can also be increased with the change of the microcontroller. Better stability will also be achieved as the circuit layout is improved.

SOFTWARE CALIBRATION

To test the software calibration method it was decided to use standard readout units instead of the prototypes above referred. A local weighing equipment manufacturer made available two 4 load cells platforms and 8 digital readout units with networking facilities. Load cells taking a maximum nominal weight of 100kg, with 3000div resolution and a sensivity around 2mV/V, were used. The 4-load cell platforms coupled to a single readout unit is rated to 200kg with a resolution of 100gr. Each of the readout units were calibrated to give around 60kg with a 20gr resolution.

To sets of tests were done one for a 4 load cells platform, and another for a 8 load cells system made approaching the two 4 load cells platforms.

The calibration method consists on doing N readings of weight on each load cell obtained by moving a mass with a known weight around the platform. The number of readings is the same as the load cells in the platform. The best results are obtained concentrating the weight as much as possible above a load cell.

For the 4 load cells platform 4 sets of 4 readings were made, and the weights found were used to workout the multiplying coefficients. These factors affecting each one of the readings, enables the correct evaluation of the weight above the platform.

A system of 4 equations and 4 unknowns was built:

$$K_1W_{11} + K_2W_{12} + K_3W_{13} + K_4W_{14} = W$$
$$K_1W_{21} + K_2W_{22} + K_3W_{23} + K_4W_{24} = W$$
$$K_1W_{31} + K_2W_{32} + K_3W_{33} + K_4W_{34} = W$$
$$K_1W_{41} + K_2W_{42} + K_3W_{43} + K_4W_{44} = W$$

The solution of this system gives the K factors required to evaluate the weight of an unknown mass.

With the following W_{rc} readings calculated with a calibrated mass of 20kg positioned in four different places:

- W_{1c} readings 3.86, 9.96, 6.82, 0.72;
- W_{2c} readings 1.74, 2.94, 10.88, 5.58;
- W_{3c} readings 4.50, 0.74, 3.54, 13.26;
- W_{4c} readings 13.30, 2.92, 1.48, 4.38;

the K_c factors evaluated:

$K_1 = 0.90025$, $K_2 = 0.91580$, $K_3 = 0.99196$, $K_4 = 0.88685$.

Using these factors several (25) weighing operations were done, with different masses (1, 5, 20 up to 80kg), located in different points of the platform, gave very encouraging results with errors bellow 50gr (4000 divisions in 200kg).

For the composite platform with 8 load cells the test was repeated and the 8 multiplying coefficients were

calculated. The weighing tests done confirmed the approach followed giving errors below 100gr, i.e. again 4000 divisions in 400kg.

CONCLUSIONS

The architecture tried had shown to be able to give the required performance at a very reasonable cost.

Further improvements are expected with the use of a new and more powerful microcontroller (PIC17C42)

Software control of the amplifier offset and gain not referred in this paper is now under promising tests using the microcontroller PWM output to vary the OFFSET and to adjust the negative feedback gain.

Once the circuit is fully tested it is planned to produce an ASIC including most of the circuit components.

Acknowledgments

We wish to thank CEL-Cachapuz Electrónica Lda, a electronic weighing equipment manufacturer, for promptly making available to us the platforms and the readout units used in this work.

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