

### TP 12.3 On-Chip Integrated CMOS Optical Microspectrometer with Light-to-Frequency Converter and Bus Interface

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This single-chip CMOS microspectrometer uses fixed-cavity Fabry-Perot etalons with optical quality and long-term stability much higher than those of tunable devices [1,2]. Many detectors are needed to cover a large optical spectral range with high resolution. Therefore, this single-chip microspectrometer contains an array of 16 addressable Fabry-Perot etalons, photodetectors and circuits for read-out, multiplexing and driving a sensor bus. This chip operates using only five external connections (including  $V_{dd}$  and  $V_{ss}$ ) covering the optical range of 400-500nm with FWHM=18nm. Frequency output and serial bus interface allow easy multi-sensor, multi-chip interfacing using a microcontroller.

The circuit and photodetectors are integrated in a conventional 1.6µm poly-silicon gate CMOS process. The basic sensor structure is shown in cross-section in Figure 12.3.1. The photodetector is a vertical pnp device, with the deep junction formed by the p-epilayer and the n-well, and the shallow junction formed by the n-well and a p+ implanted layer, normally used for the drain/source contacts (SP). Both junctions are used for photodetection and charge storage. The sensors are arranged in a 4x4 array of square photodiodes with an active area of 500x500 nm<sup>2</sup> each. Typical measured dark current is 30fA (12pA/cm<sup>2</sup>) with both junctions reverse biased at 5V in parallel.

Postprocessing consists of deposition of an Al/SiO<sub>2</sub>/Ag layer stack on top of each photodiode after completion of the CMOS process. An Al layer is used for compatibility and the Ag layer is the last step. This stack functions as a Fabry-Perot resonance cavity. The thickness of the PECVD silicon dioxide layer, enclosed between two semi-transparent metallic mirrors determines the transmission peak wavelength. The initially deposited PECVD oxide layer is thinned using four etching steps with four different masks. This results in 16 channels, each with a different resonance cavity length. Figure 12.3.2 shows measurements in transmittance indicating that each of the detectors is sensitive in only one narrow spectral band in the entire visible spectral range (400-780nm) with a FWHM of 18nm. For the 45nm-Ag and 20nm-Al layers used, maximum measured transmittance is about 15%. Only low-temperature CMOS post-processing steps are used for the fabrication of the etalons. The cavity lengths can be tuned, to cover a different spectral band, only by adjusting the etching times during postprocessing, using the same masks.

The photocurrent-to-frequency circuits feature a measurement range of 10<sup>5</sup> in light intensity level, comparable to more complex analog circuits commercially available [4]. Figure 12.3.3 shows the block diagram of the read-out circuit. It can be considered a first order (or relaxation) oscillator circuit. These circuits can be tuned over a very wide range, since only one pole (or frequency controlling element) is present [5]. Only one photodiode is connected to the comparator at a time using multiplexer  $S_1$ - $S_N$ . The voltage  $V_j$  across the junction of the photodiode varies continuously between  $V_{dd}$  and  $V_{ref}$  in a feedback loop, with the comparator, flipflops and switch  $S_{ch}$ , forming a relaxation oscillator circuit. The charge generated by the photoelectric effect directly modulates the charge across the integrating junction capacitance, thereby modulating the output frequency. The sensitivity of the current-to-frequency conversion is linear and can be calculated as:

$S_{if} = f_o / I_{ph} = 1 / (2DQ)$ . With  $DQ$  a constant, depending on the junction capacitances of the photodiode and the voltage swing across the junctions. For the photodiode described above  $S_{if} = 278$  kHz/µA (with  $V_{ref} = 2.48V$ ). The total Light-to-Frequency conversion factor is given by the product of  $S_{if}$  and the responsivity of the photodiode and the transmission of the Fabry-Perot filter.

A block diagram of the bus interface is shown in Figure 12.3.4. The Integrated Smart Sensor bus (ISS-bus) [6] is the standard bus interface. Apart from its simplicity, this bus interface has two features, suitable for microsystems. First, analog data or bitstream data can be transferred over the bus. Second, the use of Manchester encoding for transmission of the data at the logical level adds flexibility. The bus uses eight bits for addressing. The four most significant bits are used for addressing the chip, so up to 16 chips can be addressed. The four least significant bits are used to select one of the 16 photodiodes. After selection, the output frequency of the corresponding sensor is available on the bus. This timing sequence is shown on the oscilloscope plots in Figure 12.3.5.

A micrograph of the complete chip is shown in Figure 12.3.6. The die measures 4.2x3.9mm<sup>2</sup>. The analog circuits, the sensor array, the analog switches, a test diode, a metal-covered diode (for dark current compensation), a reference circuit, a reference capacitor and the comparator, are in the upper part. The bus interface, the multiplexer and some other digital circuits are shown in the lower part. Only four external connections to the chip are strictly needed:  $V_{dd}$  (+5V), ground, the clock input SCL and the bidirectional dataline (SDL), since this line can also be used for transmission of the frequency output. The other pads are the chip address pins and pins for testing. The specifications of the spectrometer are listed in Table 12.3.1.

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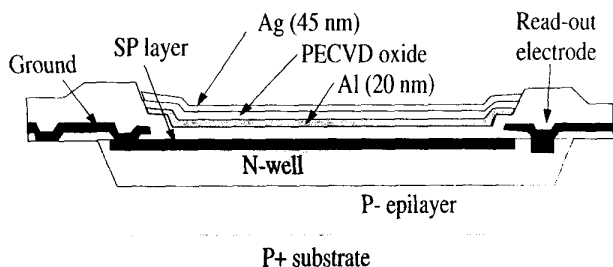


Figure 12.3.1: Photodetector structure.

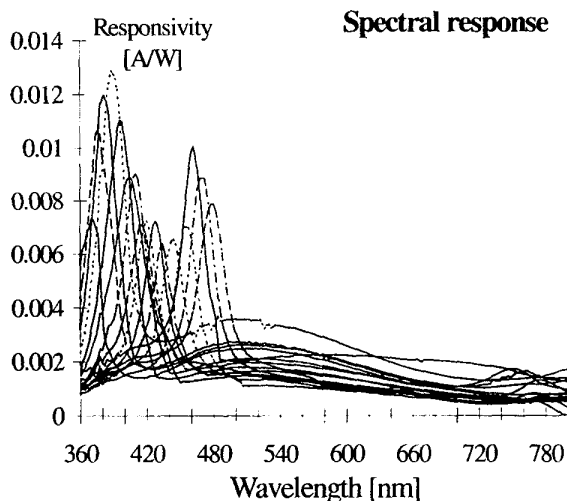


Figure 12.3.2: Spectral responses of the Fabry-Perot devices and the photodiodes.

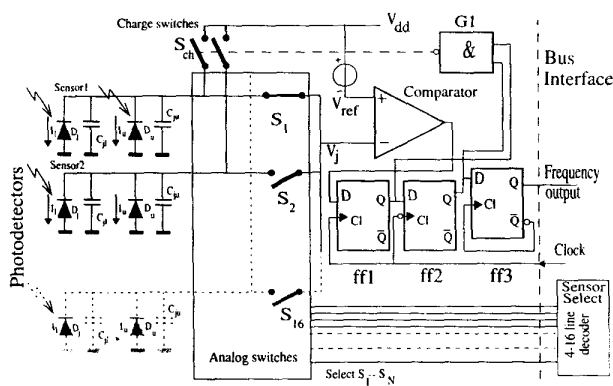


Figure 12.3.3: Read-out circuits.

Figure 12.3.6: See page 462.

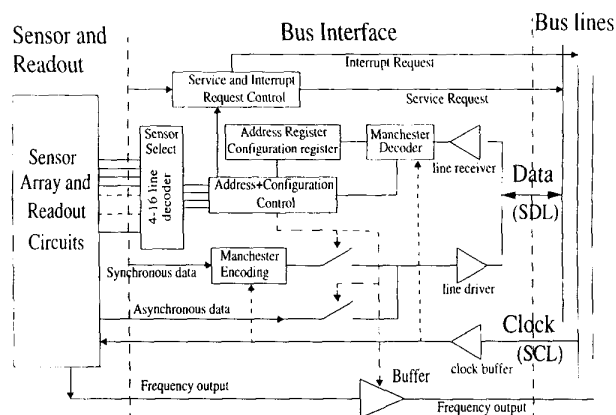


Figure 12.3.4: Block diagram of the bus interface.

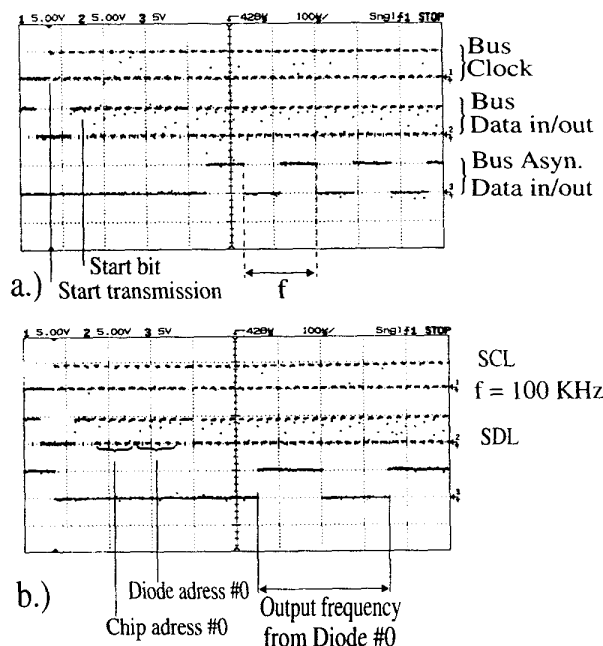


Figure 12.3.5: Oscilloscope of the bus signals: a) high light level b) low light level.

	Condition	Test result
Operating voltage	--	5 V
Power dissipation @ 1MHz	Clk= 1 MHz	1250 $\mu$ W
	Clk= 100 kHz	700 $\mu$ W
Max clock frequency	--	6 MHz
Dark frequency	25 °C	0.1 Hz
Max. frequency	Clk= 4 MHz	125 kHz
Spectral range	--	380-500 nm
Spectral resolution	--	18 nm
Responsivity	$\lambda=600$ nm	0.21 A/W
Sensitivity	$\lambda=600$ nm	75 Hz $\mu$ W <sup>-1</sup> cm <sup>2</sup>

Table 12.3.1: Chip specifications.

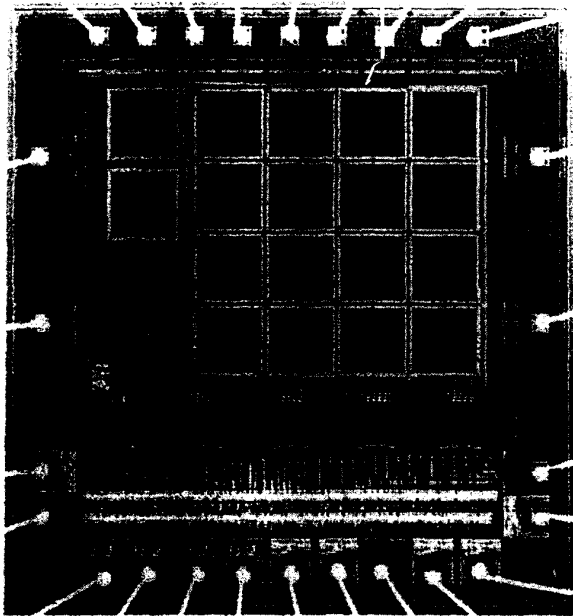


Figure 12.3.6: Chip micrograph.

General	
Circuit Area = 2.0 mm X 8.5 mm	Power Delivery = Telemetry
Power Consumption <15 mW, 4 V supply	On-Chip Power Supply = 4 Volts, Gnd
Telemetry Link	
Receiver Coil = On-chip (2.0 mm X 8.0 mm)	Range (coil-coil distance of link) = 3 cm
Transmitter Coil = Planar, air core (80 mm dia.)	Carrier Frequency = 4 MHz
Modulation Frequency = 1 kHz to 50 kHz	Modulation = ASK, Pulse width encoded
Addressability = up to 8 individually addressable devices per transmitter	
Stimulation	
Stimulation waveform = Two independent phases of opposite polarity	
Duration (each phase) = 4 to 2050 $\mu$ s (2 $\mu$ s steps)	Amplitude = 0 to 2 mA (64.5 $\mu$ A steps)
Output Channels = 8	Inter-phase delay = 12 to 1932 $\mu$ s (16 steps)
Stimulation Frequency $\leq$ 170 Hz	Maximum Output Load = 1.7 k $\Omega$

Table 12.6.1: Features.

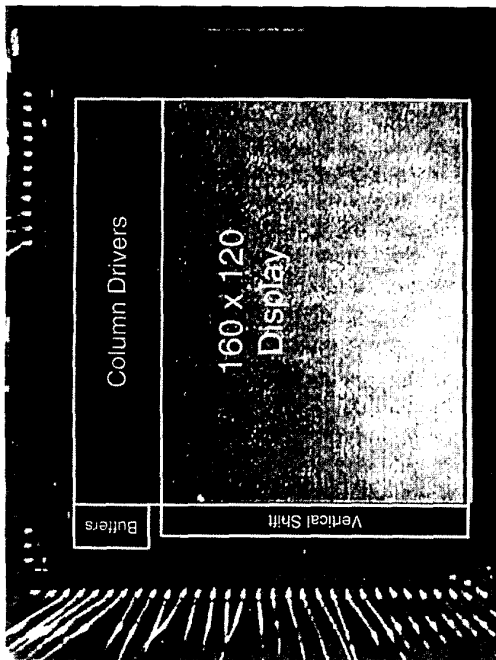


Figure 12.5.5: 160x120 display micrograph.

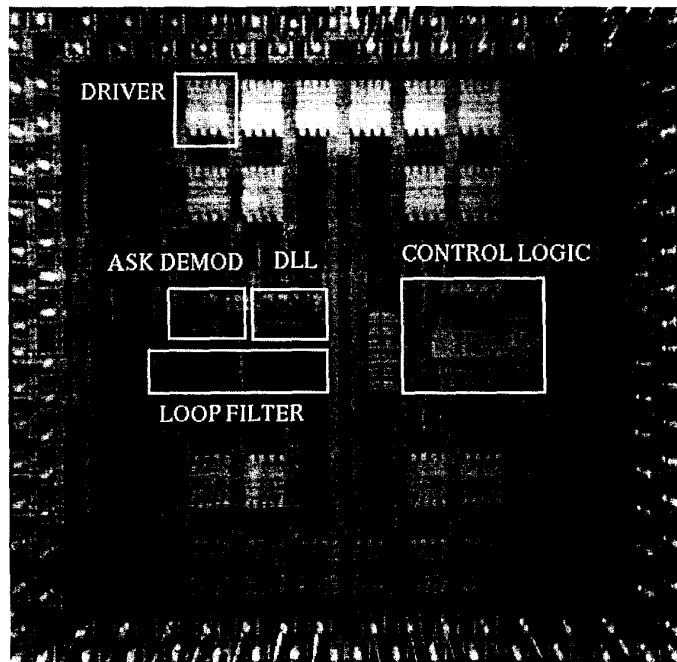


Figure 12.7.7: Die micrograph.