Special issues and methods for testing LNAs at high frequencies

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Abstract - **This paper presents the design, optimization and methods for test a high frequency high gain low-noise amplifier (LNA), using a UMC RF 0.18 µm CMOS process. The LNA was designed to be part of a low-power/low-voltage RF CMOS transceiver, for operation in the 2.4 GHz ISM band. The LNA has a power consumption of 3.6 mW, for a power supply of only 1.8 V. The LNA has a control signal that makes it to sleep in the periods when the receiver operation is not needed. These features make the LNA suitable for wireless sensor networks applications, where the low-power is a major requirement.**

I. INTRODUCTION

CMOS technology has reached its maturity. Therefore, design engineers used it for developing RF circuits. The advantages of CMOS technology are the higher integration, low-power consumption, low-voltage supply and low-cost compared with Bipolar technology. The use of CMOS process with low length for the channels of the MOSFETs is very important for high-frequency devices.

This paper describes the design and optimization of a low-noise amplifier (LNA), using the UMC RF 0.18 µm CMOS process. This process has a poly layer and six metal layers, allowing integrated spiral inductors (with a reasonable quality factor), high resistor values (a special layer is available) and a low-power supply of 1.8 V. Therefore, a high on-chip integration is possible, in favor of better repeatability as well as less pin count [1]. Without proper design, communication tasks in wireless sensors networks, may increase network power consumption significantly because listening and emitting are power-intensive activities [2]. Thus, in order to optimize power consumption, the LNA design predicts the use of a control signal. This signal makes possible to enable and disable all the LNA. Thus, it allows to switch off when no RF signals are to be received. Finally this signal can be used together with a more general signal to put the other electronics to enter in a sleeping mode.

II. LOW-NOISE AMPLIFIER DESIGN

In a typical receiver, the LNA is the first gain stage in the receiver path, thus, in a LNA, the signal must be amplified as much as possible, with a small signal-to-noise ratio (SNR) decrease. This is achieved with the best noise figure (NF).

The LNA is an inductively degenerated common source amplifier [3]. This makes the input impedance at 2.4 GHz equal to 50 Ω, for matching with antenna-switch. Cascoding transistor M_2 is used to increase the gain, to better isolate the output from input and to reduce the effect of M_1's C_{gs}. The LNA is putted in the sleeping mode, by cutting the current in the polarization stage. The same principle applies to the all subsystems of the transceiver. The inductance L_s is implemented with the bonding connection to the external PCB, which has been calculated to be 0.9 nH/mm [4]. The wires used to connect the die to an external PCB, with a RF substrate, has an inductance that adds to the LNA circuit. The use of the inductance L_{sd}, helps to reduce these effects.

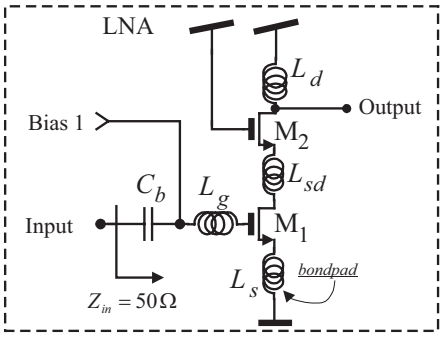

Figure 1. The block schematic of the LNA

For this LNA, the input impedance is given by

$$Z_{in} = sL_g + 1/(sC_{gs}) + [(g_{m1}/C_{gs}) + s]L_s \quad (1)$$

The input matching is made, by trimming the values of the L_s and L_g inductances. The matching is achieved, when the input impedance is real and equal to the impedance, Z_{ant} of

the antenna. The most common value is equal to 50 Ω, thus, the two following conditions must be simultaneously verified

$$\begin{cases} sL_g + sL_s + 1/(sC_{gs}) = 0 \\ (L_s / C_{gs}) g_{m1} = Z_{ant} \quad (= 50\Omega) \end{cases} \tag{2}$$

The start-up point in the LNA design, was the width calculation for the transistor M_1, using the optimal value W_{opt} [μm], given by [5]

$$W_{opt} = \frac{1}{6\pi f_c L C'_{ox} Z_{in}} \text{ [μm]} \tag{3}$$

where, f_c [Hz], is the working frequency of the LNA; L [μm] is the M_1's length, C'_{ox} [F.m^{-2}] is the oxide per area unit capacitance and finally, Z_{in} is the input impedance of the LNA, which is desired to be purely real and equal to 50 Ω.

The oxide per area unit capacitance is

$$C'_{ox} = \varepsilon_{ox}/T_{ox} \tag{4}$$

where, T_{ox} [m] is the SPICE parameter, which defines the oxide thickness [6]. The parameters, T_{ox}=4.2×10^{-9} m and ε_{ox}=4.1ε$_0$=4.1×8.85 aF/μm, presented in the UMC 0.18 μm RF CMOS process, helps to obtain the oxide per area unit capacitance, C'_{ox}=8639.3 aF.μm^{-2}=8.6393 mF.m^{-2}. Thus, the optimal width that simultaneously minimizes the consumption and the NF of the LNA, is equal to W_{opt}=284.29 μm. The UMC 0.18μm RF CMOS process has MOSFET optimized to the operation at high frequencies: the RF transistors. For such transistors, the M_1's gate-source capacitance is C_{gs}=830 fF and its transconductance is g_{m1}=20.27 mS. Finally, the values for each of the inductance are L_s=2.01 nH and L_g=3.27 nH. The most suitable block capacitance at the input of the LNA, is C_b=10 pF. The observed current at the drain of the transistor M_1 is 2 mA. This is the minimum achievable limit for the current supply.

In order to avoid mismatching problems related to the passive elements of the circuit, the design must predict as most as possible, the integration of RF components. This also applies to all DC blocking capacitors. The values of the previous inductances were obtained for a capacitance, C_{gs} for a transistor with an arbitrary width W=W_{opt}. The UMC foundry offers transistors optimized for RF operation, thus, the choice felt on these devices, due to its low-noise and better isolation properties, compared with the use of mixed-mode transistors. The width of such devices can't be any value, in fact, this value depends with the number of fingers in the MOSFETs. For each MOSFET transistor, the maximum number of fingers are twenty one (#21), e.g., the maximum width is limited to 105 μm. This was the first reason to make the width of M_1 equal to 105 μm, against the optimal value W_{opt}. The second reason, deals with the fact to have a small DC block capacitance C_b=2 pF, e.g., it occupies less chip area compared with 10 pF, thus, it's more easy to integrate this capacitor in the same die of the LNA.

The new value of the parasitic gate-source capacitances of the MOSFETs M_1 and M_2, is C_{gs}=129.94 fF. Thus, taking in account the bondwire inductance (0.9 nH/mm), it results in the internal inductance at the source of the MOSFETs, L_{s_int}=41.2 pH and with the transconductance g_{m1}=21.28 mS. These values are calculated for the drain-source voltage, V_{ds}=1.03 V and for the bias voltage V_{gs}=579 mV. Using the equation (2), it results for the external inductances, L_{s_ext}=0.264 nH and L_g=33.5 nH. It must be noted, that L_{s_ext}=L_s-L_{s_int}=R_s.C_{gs}/g_{m1}-L_{s_int}.

The gate inductance was further adjusted to a new value, L_g=21 nH, because it wasn't possible to achieve a satisfactory gain with the previous value. The purpose of the inductance L_{sd}=10 nH, is to increase the gain and to lower the return-loss of the LNA, e.g., improving the S_{11} parameter. The inductance that connects to the drain of M_2, measures L_d=4.4 nH and is tuned to the 2.4 GHz frequency by means of a 1 pF capacitance. The inductance L_s is bellow the minimum permitted by the UMC process, thus, it must be made by mean of the bondwire. The inductance L_{sd} is the only one that is not connected to the outside of the die, thus, the remaining inductances must take in account the effect of the bondwire. Then, the actual values of these inductances are slightly smaller than those obtained in the theoretical calculations. Once again, the bondwire with a diameter of 20 μm has an inductance 0.9 nH/mm [4]. The Table I shows the inductances and the quality factors of the LNA and of the bondwires [7].

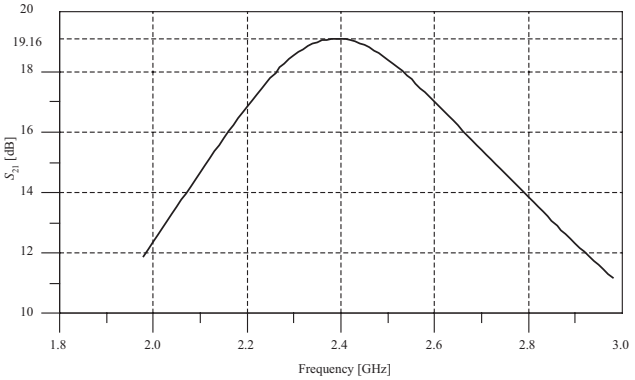

Figure 2. S_{21} parametre of the LNA.

III. RESULTS

The Figure 2 shows the S_{21} parameter of the LNA, which has been obtained with loads of 50 Ω, both connected to the input and output terminals of the LNA. It can be seen a gain above 19 dB, which is excellent for the application.

TABLE I. COMPONENTS OF THE LNA.

	Value 1 [nH]	Q_1	Value 2 [nH]	Q_2
	On-chip	*inductances*	*Bonding*	*inductances*
L_s			0.305	20
L_g	18.26	8.249	0.9	20
L_{sd}	10.00	7.177		
L_d	3.145	7.177	0.9	20

For this LNA, the S_{12} is always below -38.2 dB. This makes a good isolation from the output to the input. Moreover, the current absorbed LNA is 60 μA bellow the value for the optimal LNA, related simultaneously to the consumption and noise figure point of view. It was made an assessment to the noise figure (NF) and the results are shown in the Figure 3, where it can be seen the minimum bound of the NF, which is imposed by the technology, NF_{min} and the observed NF, NF_{LNA}.

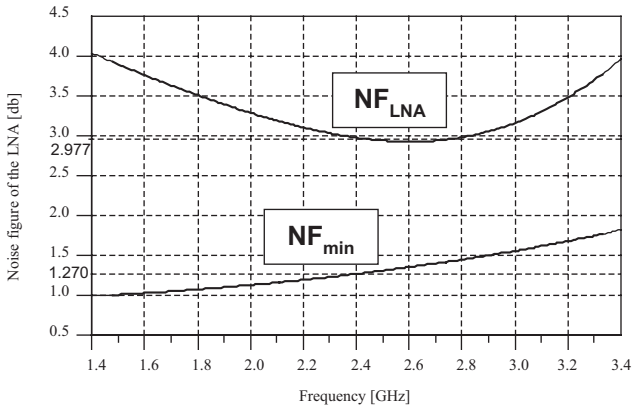

Figure 3. Noise figure of the LNA.

At the frequency of 2.4 GHz, the LNA presents the minimum value NF_{min}=1.27 dB and a noise figure of NF_{LNA}≈3 dB. The LNA is unconditional stable, with a stabilization factor, *K*, always above the unity, even for frequencies outside the 2.4 GHz neighborhood.

The power at the input of the LNA, was sweeped between the -70 dB and the +10 dBm. It was observed that the LNA stopped to amplify linearly, for input powers above the -9 dBm (IP1). As shown in the Figure 4, IP1=-9 dBm.

It was also analyzed the impact of the third harmonic, in order to get the safety bound of the LNA, which prevents the superposition of this tone with the fundamental component. As shown in the Figure 5, the superposition don't happens, if the input power is bellow -5.4 dBm (IP3).

IV. ADVANCED TESTING TECHNIQUES

A very complex problem in high-frequency testing, is the setup mounting. At the frequencies of interest, the wires used to supply these circuits and to make the measurements, presents parallel capacitances and serial inductances, which are not easy to account.

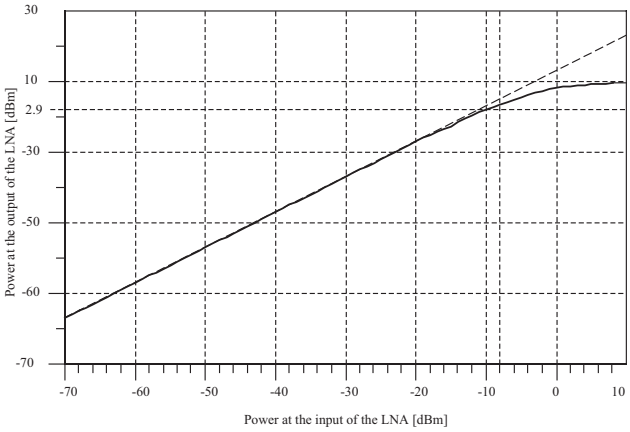

Figure 4. The 1 dB compression point (IP1) of the LNA.

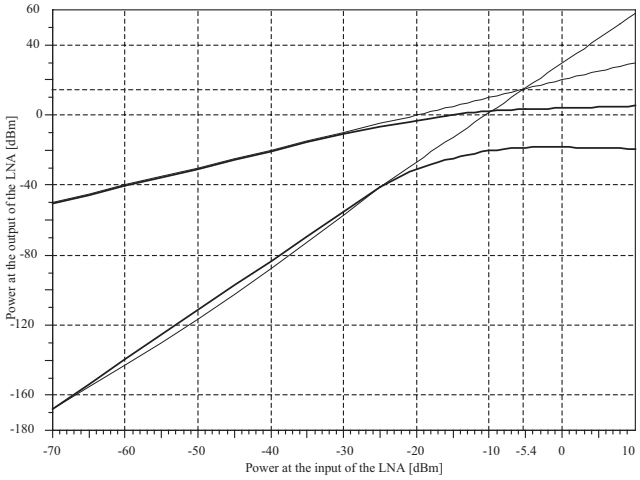

Figure 5. The 3 dB intersection point (IP3) of the LNA.

As shown in the Figure 6(a), it was included an internal MOSFET of type N, in order to create a short-circuit to the radio-frequency signal, e.g., the RF path. Thus, the RF signal don't flow across the external wires. Obviously, as shown in the Figure 6(b), the power supply must be high than the technology nominal voltage. However, this is not a problem, because the resistor R_b, placed at the output will make the supply voltage of the LNA equal to 1.8 V. To finish, Figure 7 shows a photograph of the first prototype of the microchip that contains this LNA, where it can be seen, the wires used to connect the circuits to the external PCB.

V. CONCLUSIONS AND APPLICATIONS

The design, optimization and methods for test a high frequency high gain low-noise amplifier (LNA) was presented in this paper. It was proposed a setup configuration to make the measurements independents of wires and transmission lines using to connect to/from LNA. The application of this circuit, is in RF transceivers for wireless

sensors networks, where low-power and low-voltage features are needed. The proposed method creates a RF short-circuit, which has the advantage to make use any kind of wires to make the external connections to the die, without affecting the LNA behavior.

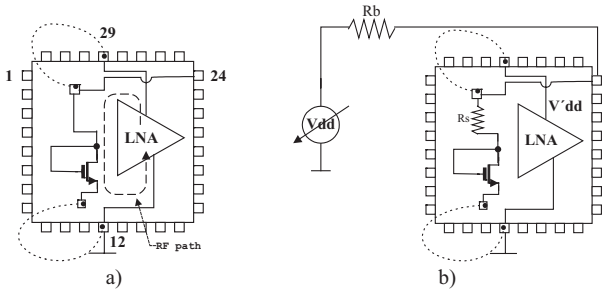

Figure 6. a) Internal MOSFET used to create a RF path, and b) illustration of the external setup, used to supply the LNA.

ACKNOWLEDGEMENTS

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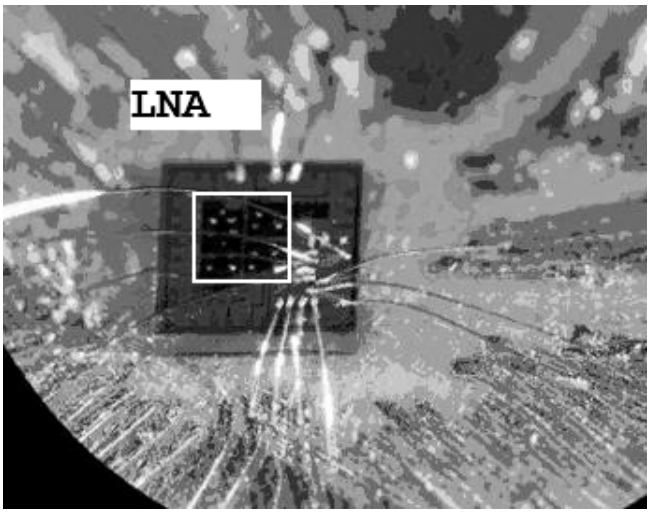

Figure 7. A photograph of the die, where it can be seen the LNA.

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