A 3.4-mW 2.4-GHz frequency synthesizer in 0.18 μm CMOS

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***Abstract* - This paper presents a low-power/low-voltage frequency synthesizer for the frequency of 2.4 GHz, which were designed and fabricated in a standard 0.18 μm CMOS process. This synthesizer is based on a Phase-locked Loop (PLL) with a integer divider in the feedback loop and for a voltage supply of only 1.8 V, it presents a total power consumption of 3.4 mW. The power consumptions for the Voltage-controlled oscillator, phase-frequency difference/charge-pump and for the divider are 2 mW, 1 mW, 420 μW, respectively. The PLL is very fast, e.g., it takes only 1.6 μs to lock, which makes it a perfect companion for devices where frequency hops must be done very quickly.**

***Keywords* - PLL, CMOS, wireless microsystems.**

I. INTRODUCTION

THIS paper presents a low-power/low-voltage frequency synthesizer as a constitutive block of a RF transceivers for operation in the 2.4 GHz ISM band, for use in wireless sensors networks. The synthesizer is a Phase-locked Loop (PLL) with a integer divider in the feedback loop, which was designed and fabricated in a standard 0.18 μm CMOS process, in order to achieve a high degree of integration, at the same time it allows to use the low-voltage of only 1.8 V to supply the chip.

II. FREQUENCY SYNTHESIZER ARCHITECTURE

The 2.4 GHz frequency carrier, is generated by means of a local oscillator, which is a Phase-Locked Loop (PLL). As depicted in Figure 1 the PLL has a reference generator circuit with a crystal based oscillator at 20 MHz (the value of f_{ref} [Hz]), followed by a phase-frequency difference circuit (PFD) without dead zone, a current steering charge pump (CP) and a third order passive filter. The passive section output is connected to the VCO, whose output is the desired frequency of 2.4 GHz. This frequency must be divided by 120 (the division ratio, N=2×30×2, at the feedback path, which is digitally selectable) and connected to the PFD again, closing the loop. The most common PLLs are those which use the integer or fractional divider ratios in the feedback path [1], In a PLL the frequency of the signal at the output is $f_{out} = N.f_{ref}$.

Special cares must be taken in order to avoid multiple values of the reference frequency [2][3]. In the case of fractional PLL, the frequency at the output changes in multiples of the reference frequency, because at each T_b[s] one pulse is removed in the feeding-back, before to be re-injected in the PFD. Of course it allows to fractionally divide the output frequency, in order to have $f_{out}=N.(f_{ref}+1/T_p)$, thus it is possible to have a more fine adjust of the frequency at the output of the PLL, but the formerly cited drawback directed the option for a integer PLL. Once presented the architecture of the PLL, further it will be described the key-topics concerning the PLL design and stability guarantee.

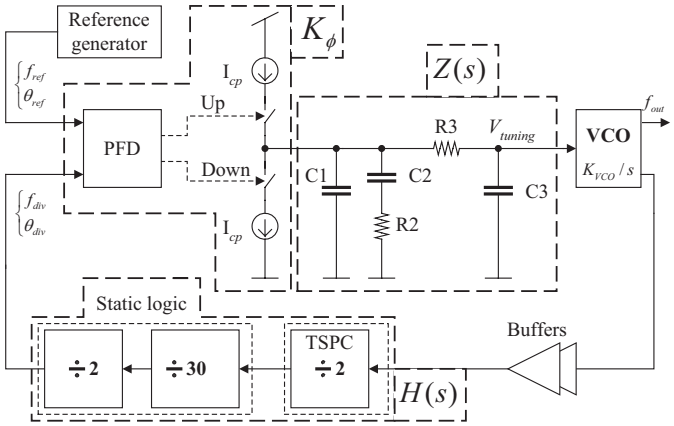

Figure 1: The structure of the PLL.

III. PLL DESIGN AND RESULTS

In conventional PFDs there is an offset around the zero phase difference, and a gain inversion region takes place for phase differences higher than 2π-Δ rad. In this gain inversion region, the PFD outputs the wrong control signals increasing the phase and frequency differences between the inputs, and the lock time takes a sudden turn for the worse [4]. The implemented PFD has a linear gain in the range $-\pi$ to $+\pi$, and a large constant gain in the range $[-2\pi, -\pi]$ and $[+\pi, +2\pi]$ [5]. This PFDs makes PLLs faster, compared to those using conventional PFDs. Figure 2 shows the schematic of the PFD.

The CP is a current steering type (see Figure 3). This circuit avoids the conventional problem in CPs, that limits the opening and closing of current sources, in fact, in spite of being switched, the current is routing from the load to an

alternative path, and from that path to the load [6]. When the control signal, $V_{control}$, is 1.8 V, the CP has a total power consumption of 1.04 mW. The currents I_{up} and I_{down} are 173 µA and 178 µA, respectively, making the detector constant gain of the CP equal to K_ϕ=175 µA/2π rad.

The circuit shown in Figure 3 is a current starved ring oscillator and it was used as voltage controlled oscillator (VCO) in the differential configuration. Its operation is similar to ring oscillators. Transistors M_9 and M_{10} operate as an inverter, while M_8 and M_{11} operate as current sources. The current sources, M_8 and M_{11}, limit the current available to the inverter. M_9 and M_{10}; in other words, the inverter is starved for current. The transistors M_6 and M_7 are mirrored in each inverter/current source stage [7]. Basically, the signal V_{tuning} imposes changes in the currents of the inverters, making them faster of lower to switch, e.g., it changes the propagations delays, τ [s]. Thus, for a N inverters VCO, the frequency of oscillation, f_{osc} [Hz], will be $f_{osc}=1/(N.\tau)=1/[N.\tau(V_{tuning})]$.

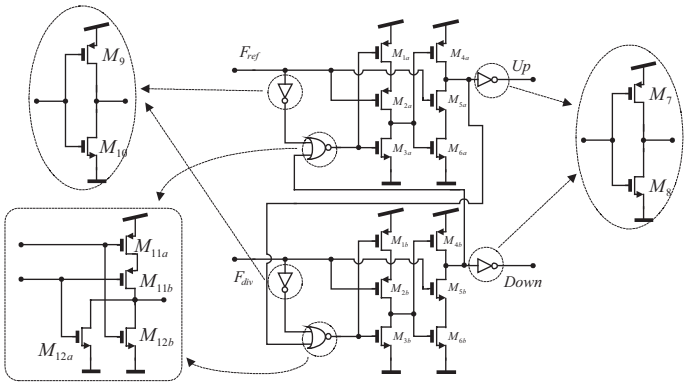

Figure 2: The schematic of the PFD.

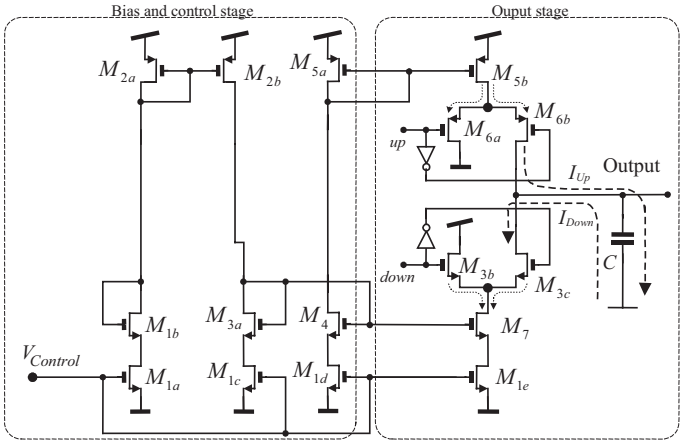

Figure 3: The schematic of the implemented CP.

Additional changes were made to the VCO presented in [7]. It was added the transistors M_7, and M_{10}. The transistor M_7 controls the whole VCO, e.g., it uses the control signal, $V_{control}$, to enable and disable the VCO. The transistor M_4 allows to keep the oscillations at the VCO, when the voltage at the gate of the transistor M_3, V_{tuning} [V], falls below its threshold voltage, V_{thn} [V] [6]. As seen in Figure 6, this makes possible to control the VCO at the full range [0, 1.8 V] for the voltage V_{tuning}. When active, the VCO has a power consumption of 2 mW.

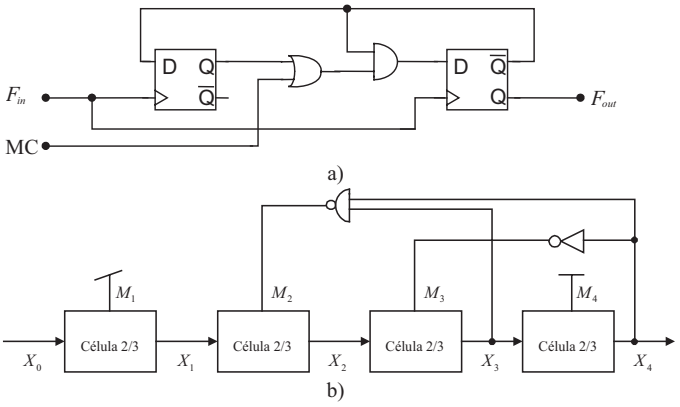

Figure 4: a) 2/3 cell with modulus control; b) frequency divider by 30.

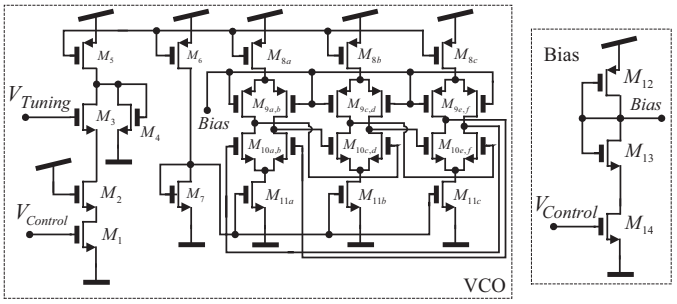

Figure 5: The schematics of VCO and bias+control.

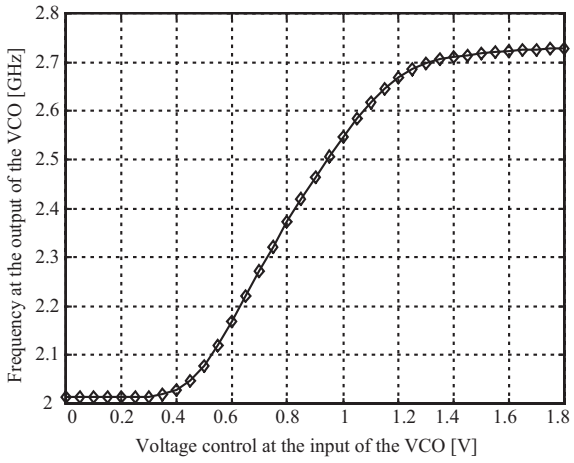

Figure 6: The working characteristic of the VCO.

The division by 120 in the feedback path is done with a cascade constituted by one half divider implemented with a true single phase clock (TSPC) logic [8], one divider by 30, followed by a toggle flip-flop to ensure a duty-cycle of 50% at the PFD input.(see Figures 1 and 4).

The TSPC logic was used to overcome the impossibility to implement the first toggle flip-flop with static logic in this technology. The results of this divider are shown in Figure 7 and it can be seen that it is required a rail-to-rail input to work properly. The ratio of 30 was achieved with the use of simple

frequency dividers by 2/3 with modulus control.

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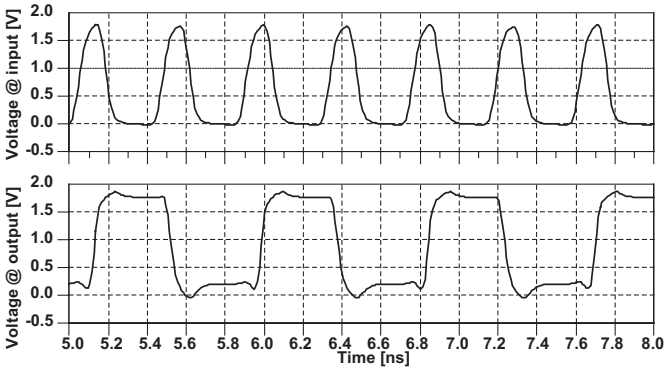


Figure 7: Waves at the input and output of the TSPC divider by 2.

IV. PLL STABILITY ANALYSIS

The ring oscillators have more phase noise than *LC* oscillators [9]. For overcoming this limitation, the bandwidth of the PLL must be high enough to "clean-up" the output spectrum around 2.4 GHz. Thus, it was used, a third order passive loop-filter (LF), composed by a second order section (C_1, C_2 and R_2) and a first order section (C_3 and R_3), providing an additional pole. The first order filter reduces spurs caused by the multiples of reference frequency, whose consequence is the increasing of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL bandwidth and below the reference. A bandwidth of approximately two times the difference between the maximum and minimum frequencies generated by the VCO was used. The stability of the loop is guarantee with a phase margin at least of $\pi/4$ rad [10].

The chose of passive components must obey to the following: given the bandwidth, f_p [Hz], the phase margin ϕ_p [rad], the minimum attenuation, A_{min} [dB], measured at multiples of the spurious reference frequency, f_{ref} [Hz], which is imposed by the low-pass filter R_3C_3, it will result in the five passive components of the loop-filter [11]:

$$C_1 = \frac{\tau_1}{\tau_2} \times \frac{K_\phi K_{VCO}}{(2\pi f_p)^2 N} \times \times \sqrt{\frac{1+(2\pi f_p)^2 \tau_2^2}{[1+(2\pi f_p)^2 \tau_1^2] \times [1+(2\pi f_p)^2 \tau_3^2]}} \quad (1)$$

$$C_2 = C_1 \left(\frac{\tau_2}{\tau_1} - 1\right) \quad (2)$$

$$R_2 = \frac{\tau_2}{C_2} \quad (3)$$

where the time constants τ_1, τ_3 and τ_2 are respectively

$$\tau_2 = \frac{(2\pi f_c)^{-2}}{\tau_1 + \tau_3}, \quad \tau_3 = \frac{\sqrt{10^{\frac{A_{min}}{10}} - 1}}{2\pi f_{ref}} = R_3 C_3, \text{ and } \tau_2 = \frac{(2\pi f_c)^{-2}}{\tau_1 + \tau_3} \quad (4)$$

From the time constant, τ_3, given in the previous equation, it seems that the components R_3 and C_3 can be any combination, since the product R_3C_3 is τ_3. However, this is not true, e.g., it is not wise to let C_3 to be higher that the other capacitances of the filter, because τ_3 ceases to be only dependent of R_3 and C_3 and becomes to interact with the other time constants. Thus, C_3 and R_3 must obey to:

$$C_3 \le \frac{C_1}{10} \quad (5)$$

$$\text{and } R_3 = \frac{\tau_3}{C_3} \quad (6)$$

The passive components were chosen with help of a custom template for the *excel* spreadsheet. Table I shows some specifications, LF components and the significant results.

For the filters listed in the Table I, the Figure 8 shows the temporal behaviour of VCO's tuning voltage, V_{tuning} [V].

TABLE I: SPECIFICATIONS, LF COMPONENTS AND MOST SIGNIFICANT RESULTS.

Parameters	Filter 1	Filter 2	Filter 3	Filter 4
Phase margin - ϕ_p [º]	45	55	45	45
Bandwidth – f_p [MHz]	1.2	1.2	1.2	0.8
Frequency f_c [MHz]	0.82	0.75	0.64	0.51
Attenuation *attn* [dB]	10	10	15	15
C_1 [pF]	10	11.7	18	35
C_2 [pF]	81	180	185	300
R_2 [$k\Omega$]	5	3.7	3.5	2.7
C_3 [pF]	1	1	1.5	3.5
R_3 [$k\Omega$]	20	20	17.5	11
Time to converge [µs]	1.60	2.94	2.55	10.40
Actual phase margin [º]	44.8	55.3	49.1	45.6
Dumping - ξ	0.76	0.86	0.81	0.79

From the previous Table and Figure, it can be seen that the PLL is very fast to converge. For this happens it was necessary to increase the bandwidth up to at least 1.2 MHz. For applications where the time to lock must be lower, it is necessary to sacrifice the phase margin, ϕ_p [rad], in order to increase the bandwidth, f_p [Hz], of the PLL.

V. CONCLUSIONS

This paper presented a low-power/low-voltage 2.4-GHz frequency synthesizer (PLL) for RF CMOS transceivers, which was fabricated in a 0.18 µm CMOS process. Thanks to its dynamic TSPC divider, the PLL has a total power consumption of only 3.4 mW. So long ago, it was demonstrated for this class of dividers, its suitableness for

multigigahertz synthesizers, since it does not impair the power supply rejection or the phase noise performance [8]. The implemented VCO has good amplitude flatness over its 44% tuning range. The PLL uses a reference signal with a frequency of 20 MHz.

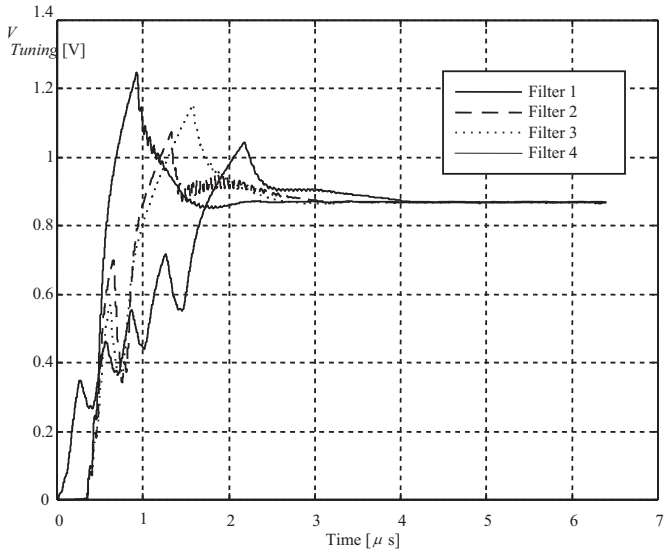
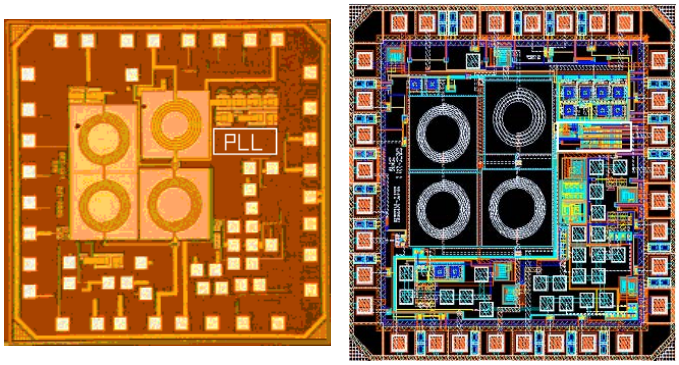


Figure 8: Behavior of tuning voltage of the VCO, V_{tuning} [V].

The Figure 9 shows a photography and the layout of the first prototype of a RF CMOS transceiver, which was designed and fabricated for use in wireless sensors applications and whose local frequency generator uses the frequency synthesizer described in this paper. The layout is shown in order to be possible to locate the PLL in the die, because the oxide below the upper metal layer (Metal 6) hides everything (the circuits).



a) b)

Figure 9: a) A die photograph showing the PLL; and b) the respective layout for a better visualisation of the PLL.

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