# High-aspect-ratio neural electrode array fabrication using thermomigration process

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## Summary

A novel fabrication process for a high-aspect-ratio recording and stimulation intracortical neural microelectrode array is described. Thermomigration performed by heat conduction is used to selectively dope a silicon wafer with aluminum and create electrically isolated paths through a back biased *pn* junction. Thin needle-shaped silicon microelectrodes are shaped with wet chemical etching process and coated with biocompatible material.

### Motivation and results

Development of neural interfaces to record and stimulate neural signal in order to assist the neurologically impaired has been a focus of bioengineering research in the last decade [1].Recent scientific advances in the neuroprosthetics therapies' field and the need to gain scientific insights on how populations of neurons interact in the complex and distributed systems that generate behavior, triggered the development for long penetrating electrodes.

Firstly the *n*-type 4 mm thick (100) silicon wafer is coated with a layer of photolithographically patterned aluminum squares, each measuring few hundreds of micrometers on a side (Fig. 1a). With the patterned side facing the cool junction and the opposite side facing the hot junction inside the furnace, a temperature gradient is created within the wafer. The aluminum squares form droplets of silicon-aluminum liquid alloy, which migrate along the temperature gradient towards the hot junction (Fig. 1b). As the droplets move through the wafer, the silicon, now doped to saturation with aluminum, recrystallizes behind the droplets. Eventually the droplets traverse the entire thickness of the wafer, and deposit themselves on the hot junction. As aluminum is a *p*-type dopant, this process leaves a trail of  $p^+$  type silicon in the *n*-type wafer [2]. The silicon wafer is diced in deep orthogonal cuts creating  $p^+$  type silicon micropillars bonded by a thin layer of *n*-type silicon at their base (Fig. 1c). These pillars are electrically isolated from each other by the resulting back to back *pn* junctions which are formed between any pair of  $p^+$  trails (Fig. 2a). The KOH etch process, sharpens the exposed  $p^+$  micropillars into pyramidal shaped needle tips (Fig. 2b). Finally an electrical contact is done in the back side of each needle and the entire array with the exception of the needle tips are protected with polyimide [3].

## References

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#### Acknowledgements

This work was supported by FCT with the reference project FCOMP 01 0124-FEDER-010909 (FCT/PTDC/SAU BEB/100392/2008).

#### Word count: 360

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// n-type Silicon

<u>*Fig. 1:*</u> Fabrication process with designs and respective photos: a) Aluminum deposition; b) Thermomigration; c) Microelectrodes array before KOH etching.



*Fig. 2:* a) Equivalent circuit between two adjacent *p*-type columns; b) Design of the final structure after sharpening the needle tips with KOH etching.