Introdução:

Conceitos básicos:

$$E = h\nu = \hbar\omega$$

$$\hbar = \frac{h}{2\pi}$$

$h = 6{,}626 \times 10^{-34}\ J.s$

$\hbar = 1.055 \times 10^{-34}\ J.s$

$m_{electrão} = 9.109 \times 10^{-31}\ Kg.$

$K_B = 8.617 \times 10^{-5}\ eV K^{-1}$

Massa do electrão no cristal e na presença de $\vec{E}$

$$m^* = \frac{\hbar^2}{\frac{d^2E}{dk^2}} = \{\text{massa efectiva}$$

O electrão livre não interage com a rede e $m^* = m_e$

A massa efectiva advém da interação do electrão com a rede devido a campos eléctricos.

Semicondutores

Estrutura cristalina e ligações

Semicondutores do grupo IV (Si, Ge, C, ...)

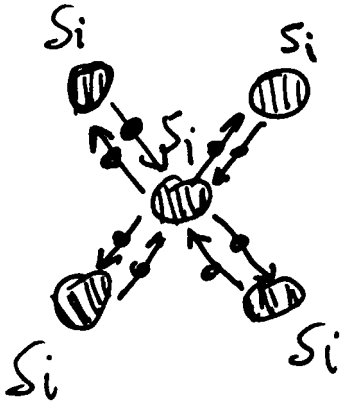
Base (motivo): 2 átomos (C, Ge, Si, ...) idênticos

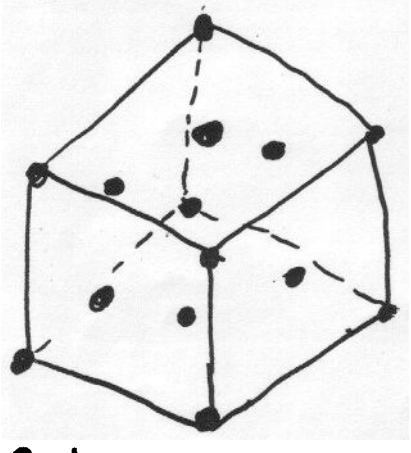
Ligação: covalente – 2 electrões (↓↑) partilhados por 2 átomos

Ex: Si ($1s^2, 2s^2, 2p^6, 3s^2 3p^2$)

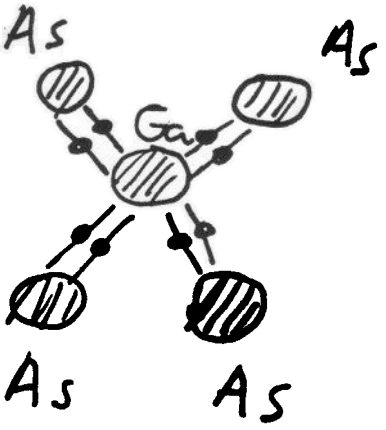
Cada átomo de Si (ligado a outros 4) contribui com um electrão para ligação (dupla)

Semicondutores do grupo III-V – contém um elemento do grupo III, outro do grupo V (GaP, InAs, GaSb, GaAs).

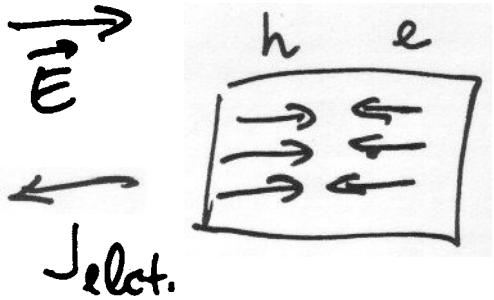




Rede cúbica de faces centradas



Condutividade Eléctrica nos semicondutores: tipo-n.



$\sigma_e = \frac{n e^2 \tau_e}{m_e^*}$ ↝ tempo de ~~recombinação~~ colisão

Valores típicos $n \simeq 10^{15} cm^{-3}$ ($10^{21} cm^{-3}$)

$\tau_e = 10^{-12}$ $\qquad \sigma = 1 \Omega m^{-1}$

$m_e^* = 0.1 m_0$

Num metal: $n \simeq 10^{28} m^{-3} \Rightarrow \sigma = 10^7 \Omega\, m^{-1}$

Mobilidade: razão entre a, v_e, velocidade dos electrões e a intensidade do campo $\vec{E}$ aplicado É a medida da facilidade com que o electrão se move na presença de um $\vec{E}$.

$$\vec{\mu} = \frac{\vec{v}_e}{\vec{E}} \quad \text{e} \quad v_e = -\frac{e \tau_e}{m_e^*} E \Rightarrow |\vec{\mu}| = \frac{e \tau_e}{m_e^*}$$

eliminando τ_e em $\begin{cases} |\vec{\mu}| = \frac{v_e}{E} = \frac{e \tau_e}{m_e^*} \\ \sigma = \frac{n e^2 \tau_e}{m_e^*} \end{cases}$

pag 18 ↳

$\sigma_e = n e |\vec{\mu}_e| = n e \mu_e$ para lacunas.

$\sigma_L = p e |\vec{\mu}_L| = n e \mu_L$

SEMICONDUTORES DE GAP DIRECTO E INDIRECTO

Transições de electrões da B.V. para B.C. dá-se por absorção de um ou mais fotões

A frequência ν do fotão tem de ser $\nu \geq \frac{\Delta E}{h}$

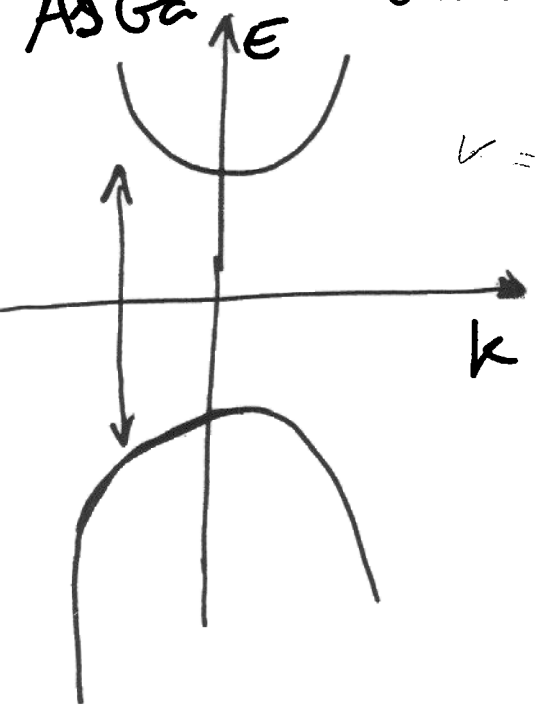
O processo passa-se com conservação da energia e da quantidade de movimento.

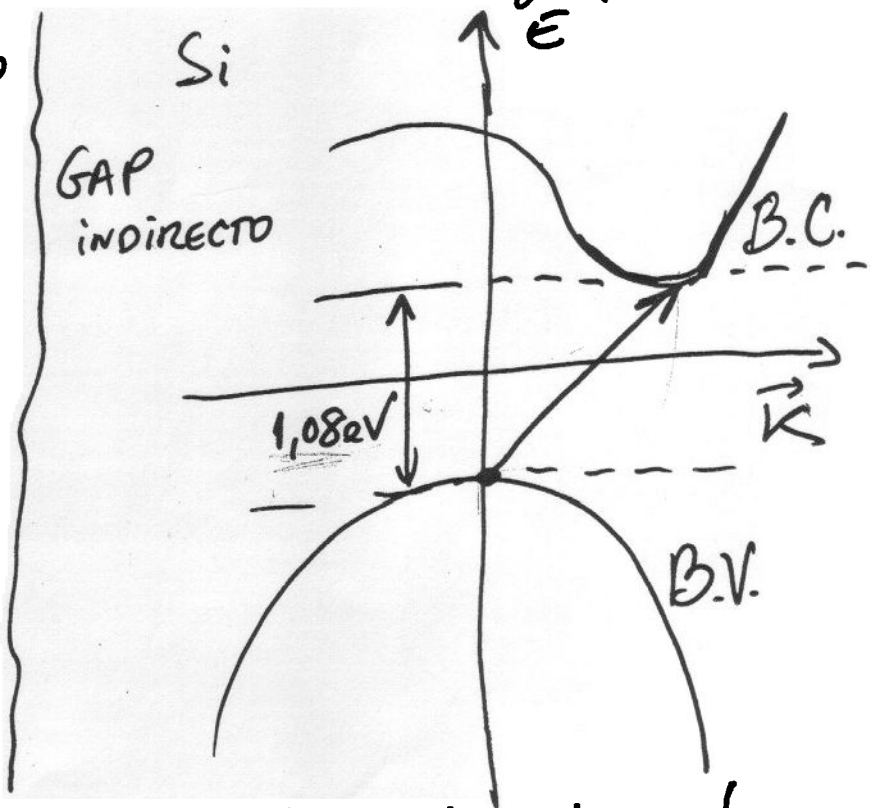
Regra de selecção: só são possíveis transições verticais (sem variação de $\vec{k}$) entre a B.V. e B.C.

e ocorre nos semicondutores de gap directo.

GAP DIRECTO

AsGa





O fundo da B.C. não se encontra directamente a baixo do topo da B.V. A transição ocorre em dois passos: i) o electrão absorve um fotão e um fonão fotão fornece a energia necessária e o fonão a quantidade de movimento ($E_{fonão} \simeq 0.05eV$).

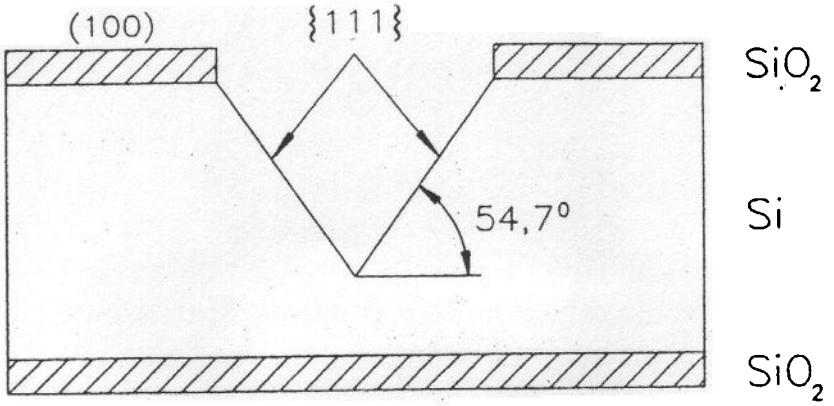


Fig. 2.7 Profile of an etched trench in (100)-silicon

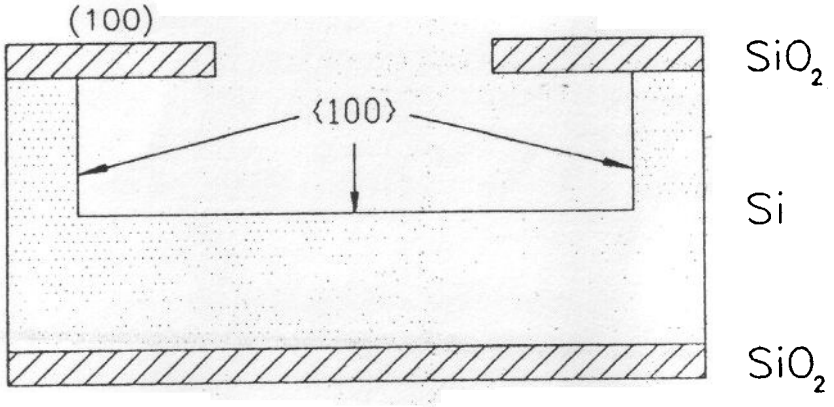


Fig. 2.8 Trenches with vertical walls in (100)-silicon

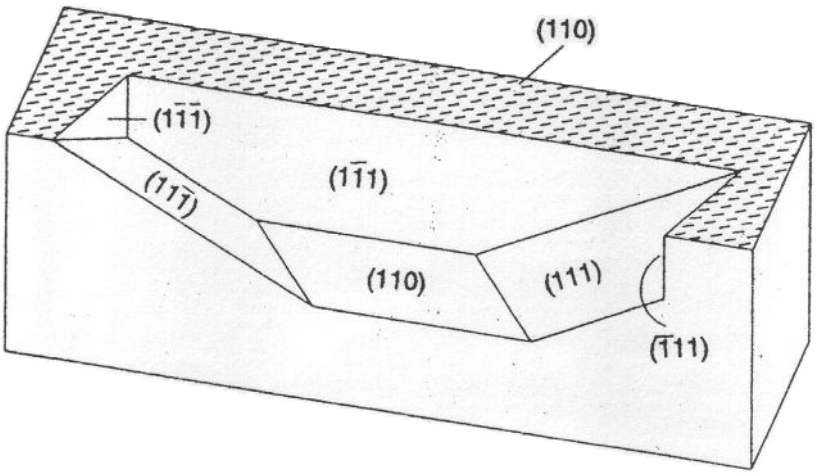
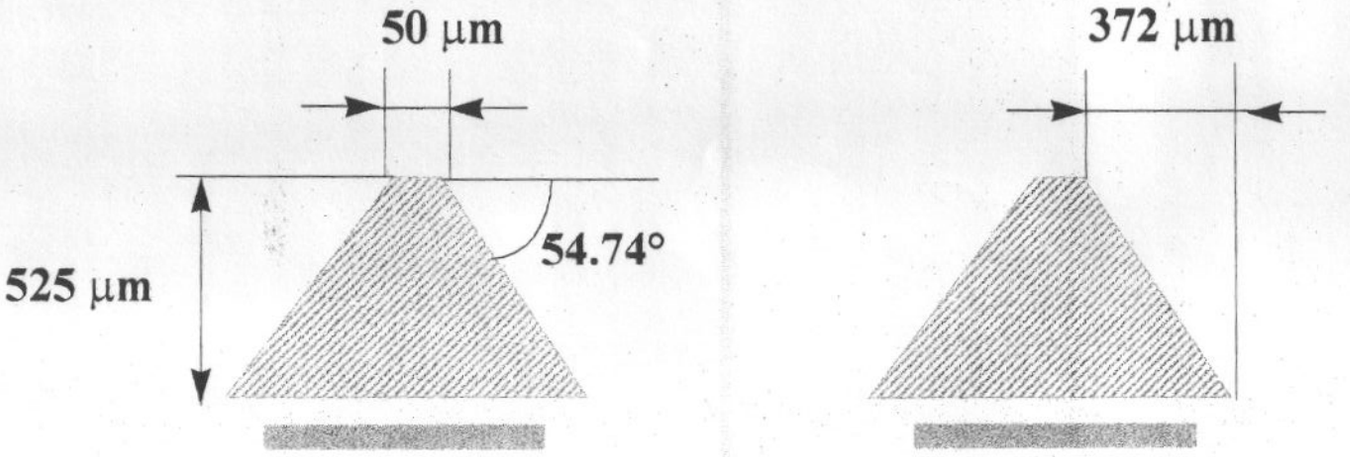


Fig. 2.9 Shapes of etched deepings in (110)-silicon

Technology implications

- anisotropic etching of silicon in KOH
- corner compensation structures
- material data extracted from the fabrication process



CMOS PROCESS TECHNOLOGY

Process Features

The CMOS01 process is a 1.6 µm Poly Silicon gate CMOS technology.
It uses a 12 µm p-type epi layer on four inch low ohmic p-type substrate wafers. The n-channel device is made directly in the epi and the p-channel device is made in an N-well. For the n-channel devices precautions are taken (Ldd implants) to prevent hot electron gate oxide degradation mechanisms.

Some further characteristics:

Single Poly		
Double Metal		
Gate Oxide Thickness	:	25 nm
Minimum Gate Length	:	1.6 µm
Minimum Pitch for Metal 1 and Metal 2	:	4.8 µm
Minimum Pitch for Poly Silicon	:	4.0 µm
Nominal Supply Voltage	:	5.0 V
Maximum Ratings	:	-0.5 to 6.5 V
MOS Transistors W/L=20/1.6 @ 27 °C		
Threshold Voltages, typical values		
Vt_n		0.75 V
Vt_p	:	-1.10 V
Saturation Currents @|Vds|=5V, |Vgs|=5V, |Vbs|=0V		
Ids,sat_n	:	4.75 mA
Ids,sat_p	:	1.90 mA

Process Flow

The eMOS01 process is a conventional CMOS process, based on LOCOS. In the following cross sections the process flow is shown for the construction of a basic CMOS inverter, if the masks NW, OD, NWI, PS, SP, SN, CO, IN, COS and INS are applied. For a detailed definition of these mask names see chapter 4.

Short desription of the subsequent process steps:
The starting material is a p-type substrate with a 12 µm epitaxial layer.
A 660 nm thick oxide is grown and NW areas are defined. Phosphor is implanted and the masking oxide layer is removed. Now the pad oxide stack, consisting of 40 nm oxide and 100 nm nitride is defined by the OD mask.
Before growing the LOCOS oxide an NWI mask is applied. The NW region is masked by both the pad oxide stack and the photoresist layer and this is thick enough to protect the NW for the two following boron implantations. The first one with low energy is the (parasitic) channel stopper, which is only present outside the pad oxide stacks. The second implantation with high energy is the n-channel anti punch through implant. Due to its high energy the boron implant can cross the pad oxide stack.
Now the LOCOS oxide is grown and the pad oxide is removed. A 25 nm gateoxide is grown followed by a boron threshold adjust implant. Now poly silicon is deposited, which is made low ohmic by phosphorous doping and the transistor gates, poly silicon resistors and poly tracks are defined by the PS mask. The SN mask is applied and a phosphor implantation forms the ODN+ areas for the source or drain of n-channel MOSTs and N+ resistors. A gate spacer technology is used consisting of a deposited TEOS oxide layer, which enables the formation of a so called D(ouble)D(iffused)D(rain) or L(igthly)DD. The SN mask is applied again and the second implant is arsenic. Now the SP mask is applied and boron is implantated, which forms the ODP+ areas for the source or drain of p-channel MOSTs and P+ resistors.

The previous steps are defined as front-end processing and all the semiconductor devices are made. What rests is 'just' the connection between them and to the outside world. The following steps are called back-end processing.

A 100nm TEOS layer and a 600nm B(oron)P(hosphor)S(ilicate)G(lass) layer are deposited. The latter is reflowed to planarize the topology. The CO mask is applied and contact windows are etched to reach ODN+, ODP+ and PS regions. The wafer is covered with aluminium and the IN mask defines the first interconnect layer. Then plasma oxide is deposited, which serves as insulating layer. The COS mask is applied and contact windows are etched. The wafer is coverd again with aluminium and the INS mask is applied to define the second interconnect layer. On request the last step in the process can be the deposition of a scratch protection layer, which requires the CB mask for definition of the contact openings to the bondpads.

Devices

Device Types

The following devices are available in the CMOS01 process :

Transistors

n-channel enhancement MOS transistor
p-channel enhancement MOS transistor
vertical pnp transistor (poor man's bipolar)

Diodes

n+/p- junction diode (ODN+/SUB)
p+/n- junction diode (ODP+/NW)
n-/p- junction diode (NW/SUB)

Resistors/Conductors

Poly Silicon resistor (PS)
Diffused resistors (ODN+ and ODP+)
N-Well resistors (NW)
First metal resistor (IN)
Second metal resistor (INS)

Capacitors

IN-PS plate capacitor
INS-IN plate capacitor
INS/PS - IN sandwich plate capacitor
PS-ODN+ capacitor

Other resistors and capacitors should not be used. They are just parasitic elements, which are not explicitly monitored and have values that can change due to process variation.

Mask Names

The following mask names are reserved and can not be used for other purposes than indicated.

Coding masks for the circuit designer to use:
NW - N-Well definition
OD - Oxide Definition for creating active area
PS - Poly Silicon definition
SP - Shallow P, P+ implantation definition
SN - Shallow N, N+ implantation definition
CO - COntact window definition of IN to OD or IN to PS
IN - INterconnect definition of first metal layer
COS - COntact window Second, definition of via from INS to IN
INS - INterconnect Second, definition of second metal layer
CB - Contact window Bondpad, definition of scratch protection openings

Additionally the following "software" masks can be specified to explicitly define the functionality of the layers underneath:
This may be useful for layout extraction programs.
GRN - Guard Ring N, NW/N+ definition
GRP - Guard Ring P, P+ definition
RNW - Resistor NW definition
RPD - Resistor Poly or OD definition

Physical masks, used for mask making:
NW, OD, NWI (*), PS, SP, SN, CO (**), IN, COS, INS, CB.
(*) Inverse NW mask. Necessary because only one type photoresist is used.
(**) Note that the CO mask can be a merged mask from the three different contact types CON, COP and CPS as specified below.
CON - Contact hole for connection of IN with ODN+
COP - Contact hole for connection of IN with ODP+
CPS - Contact hole for connection of IN with polysilicon

Mask Numbering

In general the following convention is used for the numbering of the masks in a Gds2 output layer file

Gds2 number:	in use for:
0-40	masks
41-51	plottext, pattern frame
52-62	for special use
63	bulk

Definition of mask numbering in Gds2 for the DIMOS01 process:

Gds2 mask name	Gds2 mask number	inverted y/n	total grow[µm]
NW	10	n	0
OD	7	y	1.2
NWI	10	y	0
PS	3	y	0.30
SN	6	n	0
SP	9	n	0
CO	11	n	0
IN	2	y	0
COS	21	n	0
INS	22	y	0
CB	16	n	0
CON	31	n	0
COP	32	n	0
CPS	33	n	0
RPD	35	n	0
RNW	36	n	0
GRN	38	n	0
GRP	39	n	0

There are special mask layers, e.g. plottexts, which are not used for making physical masks.

Gds2 mask name	Gds2 mask number	in use for:
PTODN	41	plottext attached to OD
PTPS	42	plottext attached to PS
PTIN	43	plottext attached to IN
PTINS	44	plottext attached to INS
BB	40	Bounding box

4.3 Layout design rules

Definitions used in the layout design rules

thin oxide	-	OD covered with PS.
OD N^+	-	OD covered with SN.
OD P^+	-	OD covered with SP.
cold N-well	-	N-well connected to the most positive voltage (VDD).
hot N-well	-	N-well not connected to the most positive voltage.
cold diffusions :		
outside the N-well	-	a diffusion which has the same potential as the substrate.
inside the N-well	-	a diffusion which has the same potential as the N-wel
hot diffusions :		
hot N^+ diffusion	-	all N^+ diffusion regions outside the N-well which have a potential not equal to the substrate voltage
hot P^+ diffusion	-	all P^+ diffusion regions inside the N-well which have a potential not equal to the N-well potential.

Terminology and numbering used in the layout design rules

0. general rule without specification of geometry in µm.

1. width or dimension of A

2. space between two regions of A

3. overlap of B over A (in all directions)

4. separation from A to B

5. extension of A edge beyond B edge (in 1 or more directions)

6. extension of A region inside B region (in 1 or more directions)

7. rule for the specified layer, concerning other masks

Note: All specified geometries must be interpreted as Dimensions On Silicon.

Level : NW - N-Well

NW.1.1	The dimensions of NW are determined by other rules, however the minimum dimensions are	A 8.0 µm
NW.2.1	Minimum space between two NW regions with at least one not connected to VDD (hot well)	B 12.8 µm
NW.2.2	Minimum space between two NW regions, both connected to VDD (cold wells) Merge if spacing is less.	C 8.0 µm

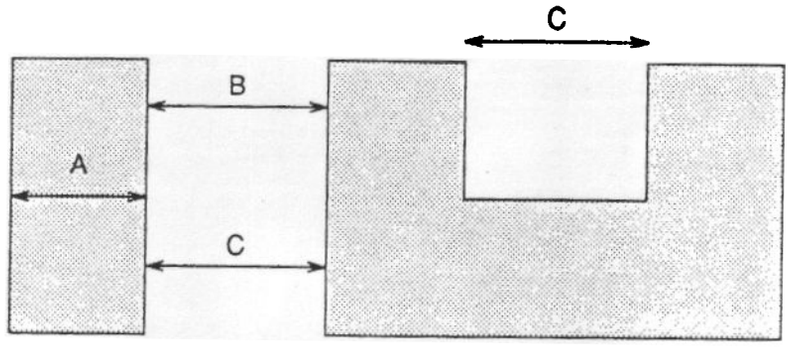


Figure 4.3.2. NW Design Rules

Level : OD - Oxide Definition

OD.0.1	OD areas have to be covered with either SN or SP (see SN and SP rules)		
OD.1.1	Minimum OD width for interconnect	A	1.6 µm
OD.2.1	Minimum space between two OD regions (both regions are inside or outside an N-well)	B	3.2 µm
OD.3.1	Minimum NW overlap over OD P+	C	4.8 µm
OD.3.2	Minimum NW overlap over OD N+ (N-well contact)	C	0.0 µm
OD.4.1	Minimum separation from OD N+ to a cold N-well	D	4.8 µm
OD.4.2	Minimum separation from OD N+ to a hot N-well	D	9.6 µm
OD.4.3	Minimum separation from OD P+ to NW (substrate contact)	E	4.8 µm

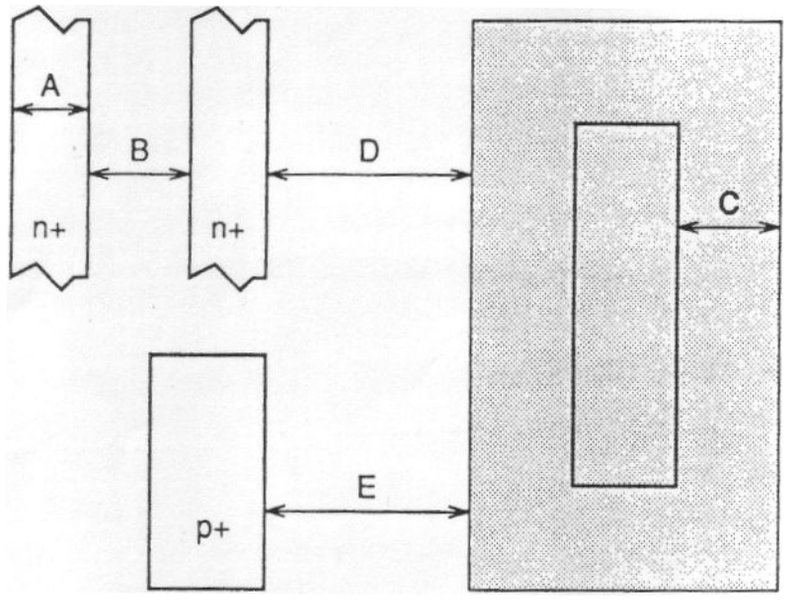


Figure 4.3.3. OD Design Rules